New Tests of Prototype CDS chip

E.Barrelet, J.F.Genat, A.Secroun, R.Sefri *LPNHE, Paris*

1 General

The prototype Correlated Double Sampler (CDS) chip was designed by Carl Grace in summer 1999, translated to DMILL 0.8 μ technology by Jean-François Genat with the support of the LBL group, submitted in December 2000 and delivered in June 2001.

The aim of this project, besides proving the feasibility of the integration of a full CCD analog readout on one chip, is to measure the relevant figures of merit of the DMILL radhard process and to check the integration of the classical CDS circuitry.

Some problems appeared during a first round of tests (September to November), notably a high chip mortality which seems to be cured by wire bonds potting technique applied to our last chips. More important the practical limitations of "standard" oscilloscope measurements led us to install a new test setup around Christmas.

This paper present our new test setup and its first results and to compare them with our electronic simulations.

2 Description of the CDS prototype and its test setup

2.1 Role of the CDS in the CCD readout chain

In Figure 1 only half of the CDS circuitry is shown. The second half, dealing with the
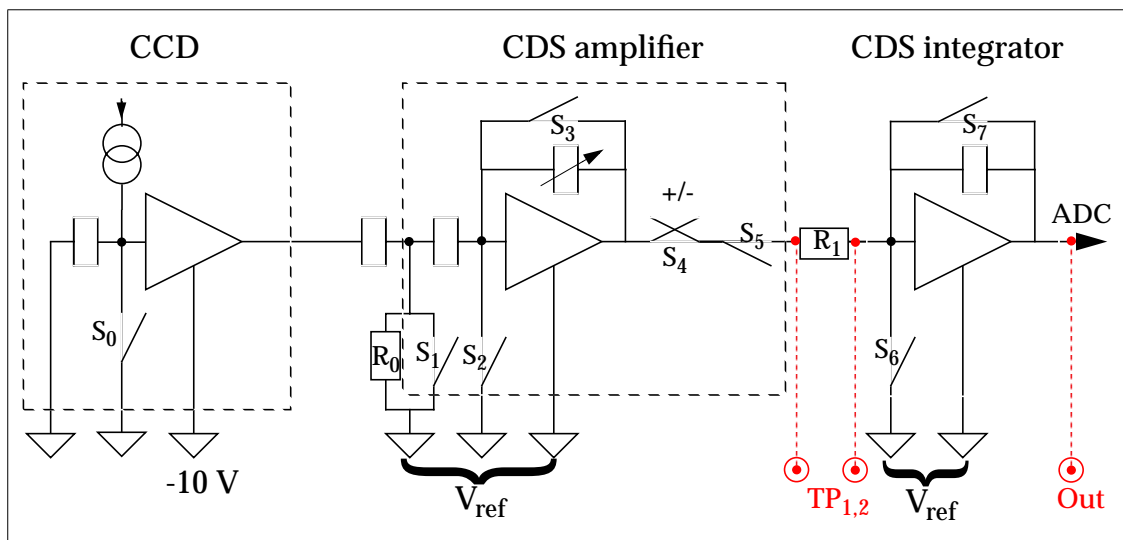

Figure 1: Simplified description of the CDS role in the CCD readout chain. (S_0= CCD reset, S_1= clamp, S_2&S_3=amplifier reset, S_4= polarity exchange, S_5= integrator gate, S_6&S_7= integrator reset)

opposite signal polarity, is integrated in the same chip than the first, but it has its own input and output pads, its test points, its reference voltages and clock signals. For each polarity

there are 5 pairs of clocks controlling the 7 switches shown in Figure 1 (switches S_2 and S_3 are controlled by the same "amplifier reset" clock and S_6 and S_7 by the same "integrator reset" clock). The CDS chip is bonded on a printed circuit which contains line receivers for each clock and decoupling capacitors for the power supplies.

The CDS chip is producing internally, for each signal polarity, current sources at intermediate voltages between 0 and V_{DD}, named V_{B1} to V_{B4}, which are accessible on CDS output pads.

There are two connections between the two mirror halves of the CDS circuit:

1. The switches S4 which exchange the polarity of the signal seen by an integrator between the first phase ("baseline after reset") and the second ("charge sensing") of a CCD pixel measurement, thus yielding the "analog subtraction" of the baseline.

2. The feed-back mechanism, shown in Figure 2, which acts on the current sources
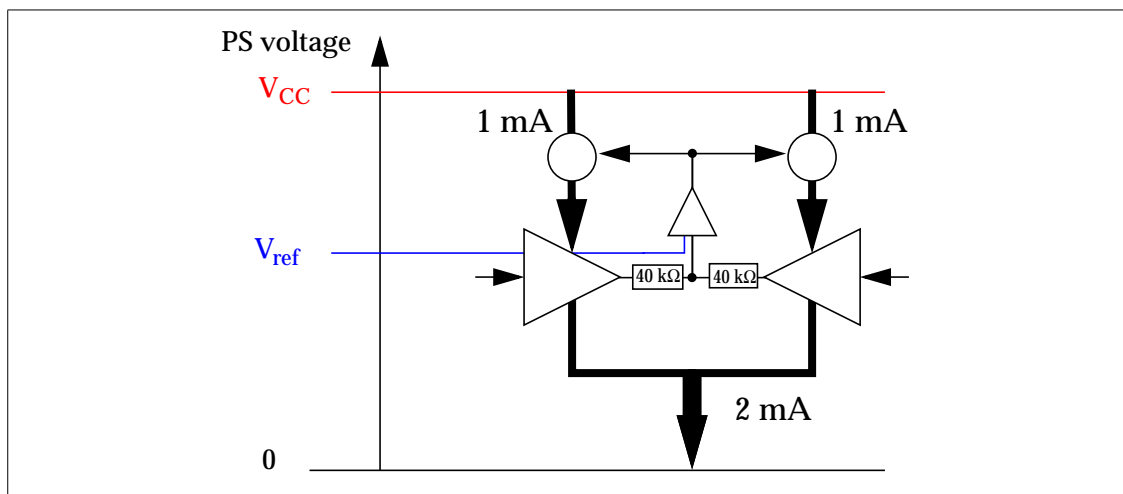

Figure 2: Feed-back system for the amplifier biasing level: the average of the two DC output levels of the two amplifiers of opposite polarities is maintained constant and equal to a V_{ref} value (generated inside the CDS chip), by feed-back on the current sources powering both amplifier.

which power the 2 amplifiers (and the 2 integrators) in order to yield a constant average value of both signal polarities.

2.2 The new test setup

Our setup:

1. generates a clock sequence using NIM electronics, (NIM signals are either converted to TTL clocks or they trigger some pulse generators),
2. digitizes both outputs of the CDS amplifier or of its integrator at a 1 Gsample/s rate using a "Digital Signal Analyser" (Tektronix DSA 602 with 2x2 11A32 inputs),
3. accumulates under LabView a good statistical sample (e.g. 1000 waveforms),
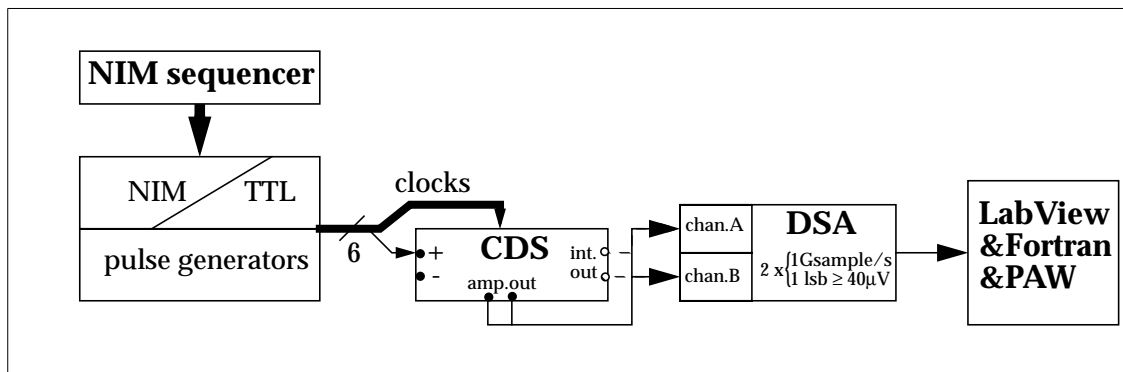4. analyses the data with some classical HEP statistical tools.

Figure 3: New test setup (january 2002)

The main advantages are:

1. no obvious frequency limitations (400, 100 and 20 Mhz choice of DSA input filters)
2. not much noise ($5nV/\sqrt{hz}$ white noise)
3. possibility to subtract from each waveform a non reproducible complex baseline and to compare several consecutive CCD readout cycles)
4. possibility to simulate the effect of various filters on experimental data

3   Present Status

We have completed a set of basic tests described hereafter, after solving empirically a few technical problems left for further analysis.

3.1   Linearity, gain and range of CDS amplifier

Linearity is checked at the 1% level which is the limit of our digitizer measurement within the ±1.5 V range predicted by our electronic simulation (cf.Figure 4).

. The only discrepancy with the simulation is the absence of a flat saturation level at 1.8 V.

The ratio of gains is also well consistent with the nominal gain values, i.e. the ratio of the feed-back capacitances designed by the CAD of the DMILL process.

3.2   CDS amplifier noise

The CDS amplifier noise is studied by digitizing output waveforms (test point TP1 in Figure 1) when 50 Ω are connected to both inputs and the only active clock is the "amplifier reset". As one can see inFigure 5 a) , the baseline has an exponential shape between two resets. The extraction of this baseline by a quadratic fit (cf. Figure 5 b), procedure separates the high frequency noise (gaussian on a 4 order of magnitude range as shown in Figure 6,a) from the low frequency noise coming from the reset switches S2 and S3 and from the AC pickup (cf. Figure 6 b). These two LF components are separated respectively by taking the difference and the sum of the baseline fitted for 2 consecutive reset periods.
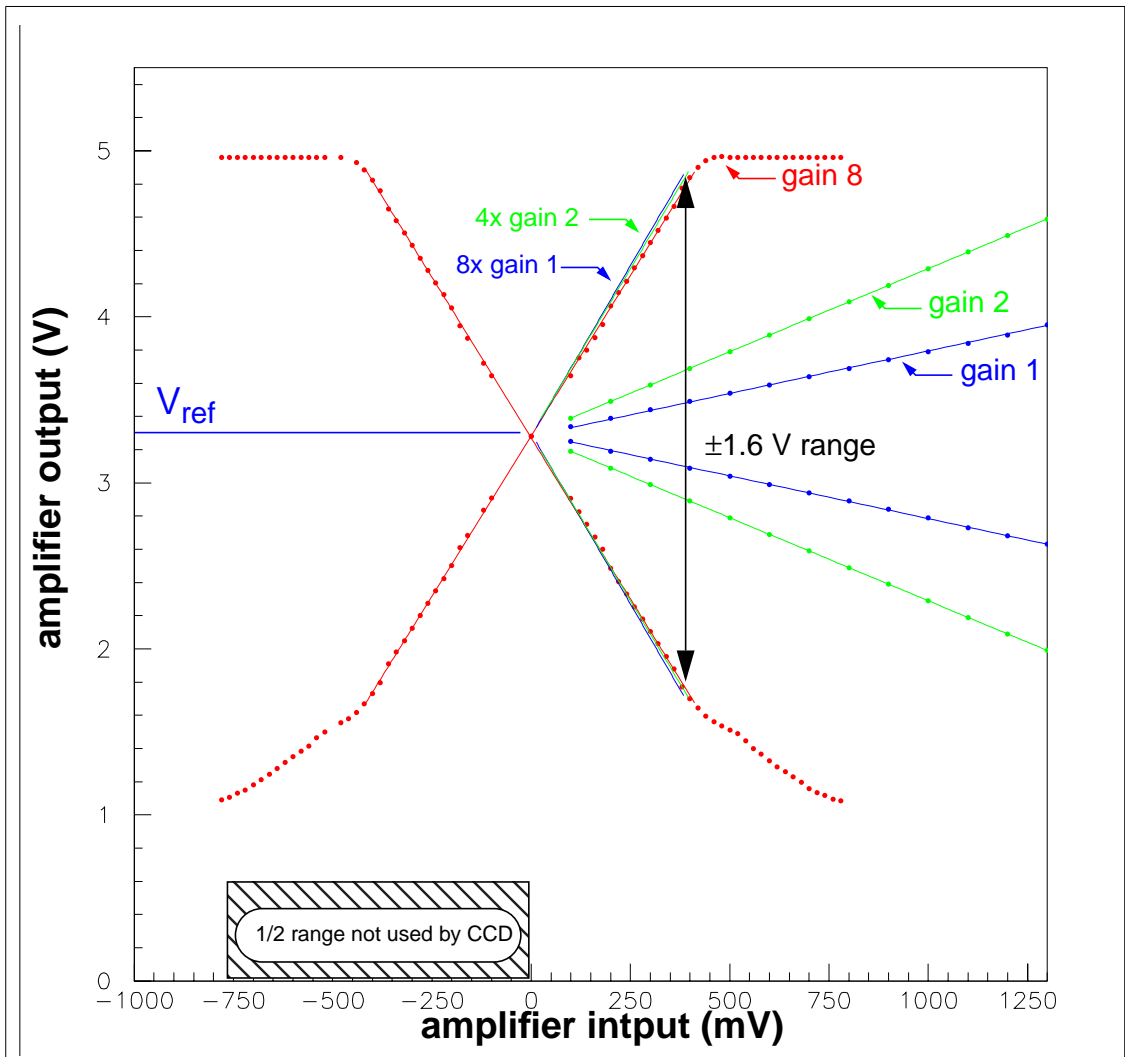
Figure 4: Transfer function of the CDS amplifier at various gain

3.3 Gain and range of CDS integrator

Because of stability problems at higher gains, we used only one amplifier gain equal to 0.5. In this condition, an overall gain 1 for the full chain is obtained for T_{int}= 8 µs as seen in Figure 7. This is entirely consistent with the design value T_0= 4 µs, designed to get an overall gain 1 at $T_{int}=T_0$ for an amplifier gain equal to 1.

$$G_{overall} = G_{amplifier} \times \frac{T_{int}}{T_0} \qquad T_0 = 4\mu s$$

3.4 CDS integrator noise

Following the technique used in Section , we made two 2 µs wide time-windows in a period of 20 µs between two integrator resets -one before the arrival of the signal and the other one any time after, as shown on Section Figure 8:.
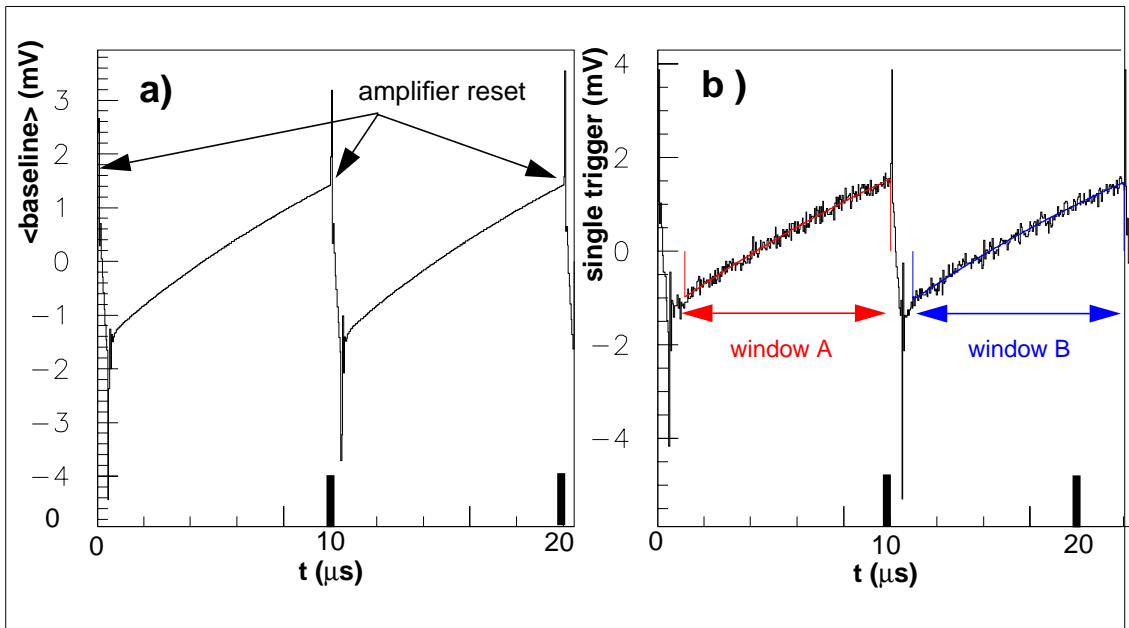
4

Figure 5: Components of CDS amplifier noise are extracted by digitization of 2 periods following 2 consecutive amplifier resets. Figure a) is obtained by averaging 1000 waveforms. For each window A and B where the baseline is stable, each waveform can be fitted as shown in b) by a second degree polynomial approximating the real exponential behaviour (time constant = 20 ms). The residual of this fit yield the high frequency component of the noise. The parameters of the fit yield the low frequency components..
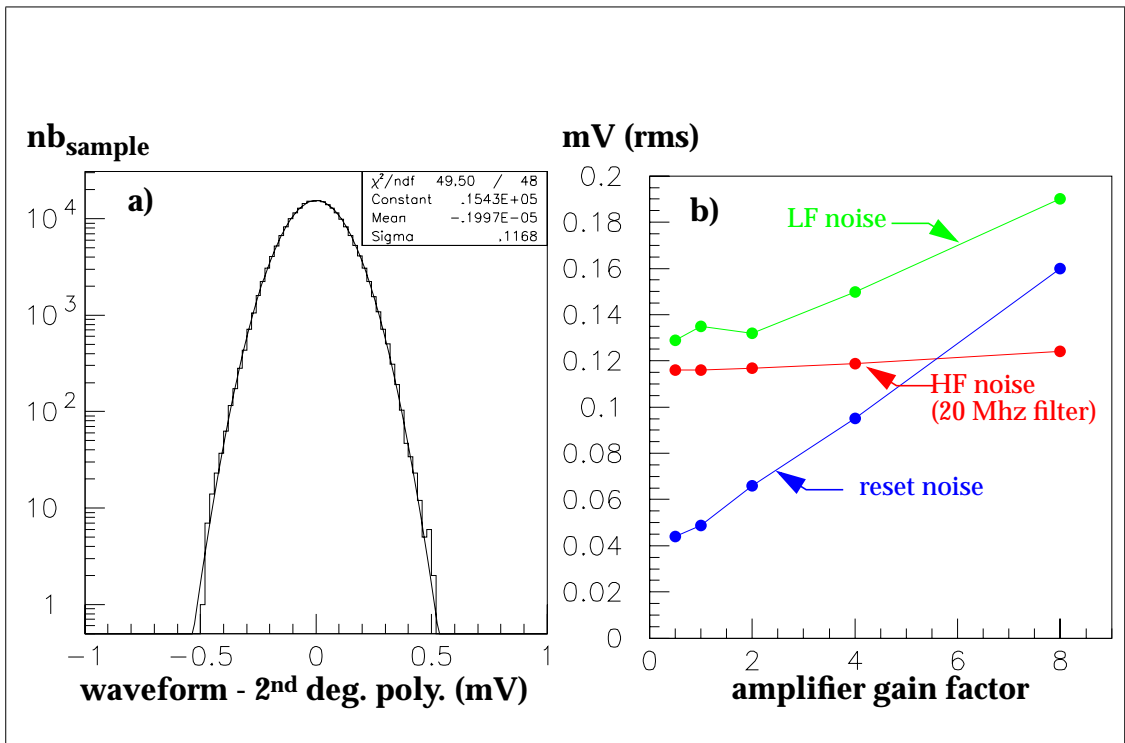

Figure 6: a) High frequency noise, extracted as shown in Figure 5, is gaussian on 4 orders of magnitude, b) behavior of the components of amplifier noise as a function of gain.
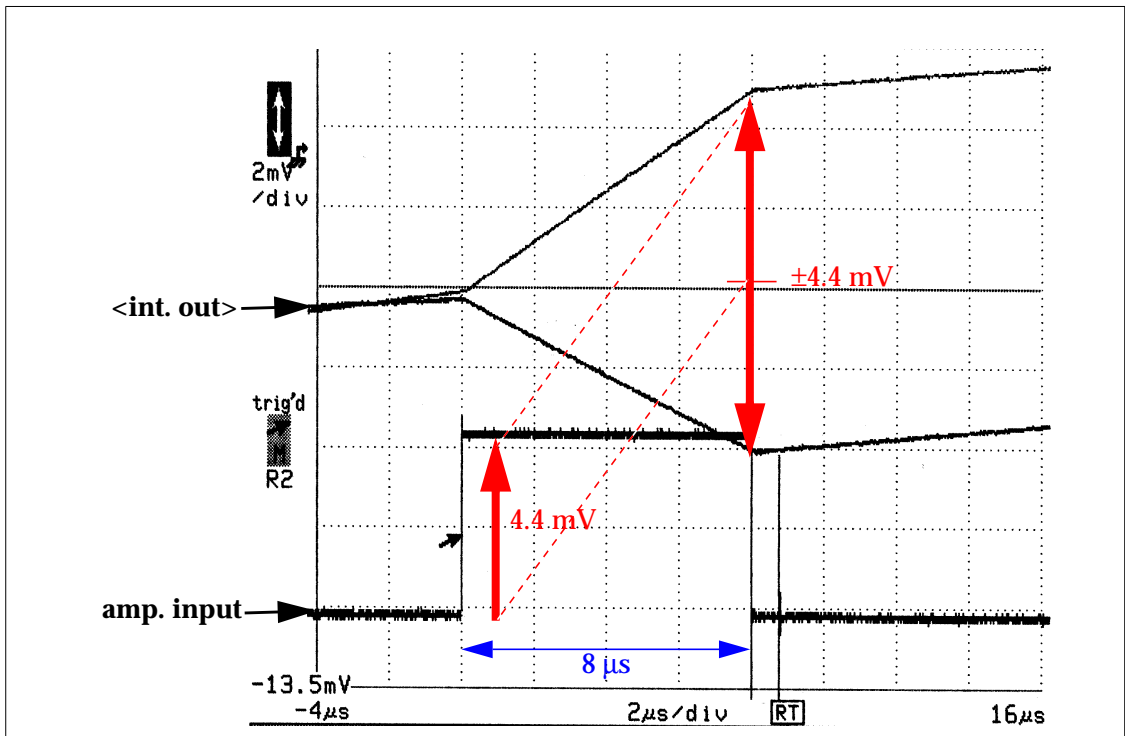
Figure 7: Check of the calibration of the overall gain of the CDS: the amplifier input is compared with the 2 integrator outputs. The outputs have been averaged to get rid of the noise. The amplifier gain is 0.5.f
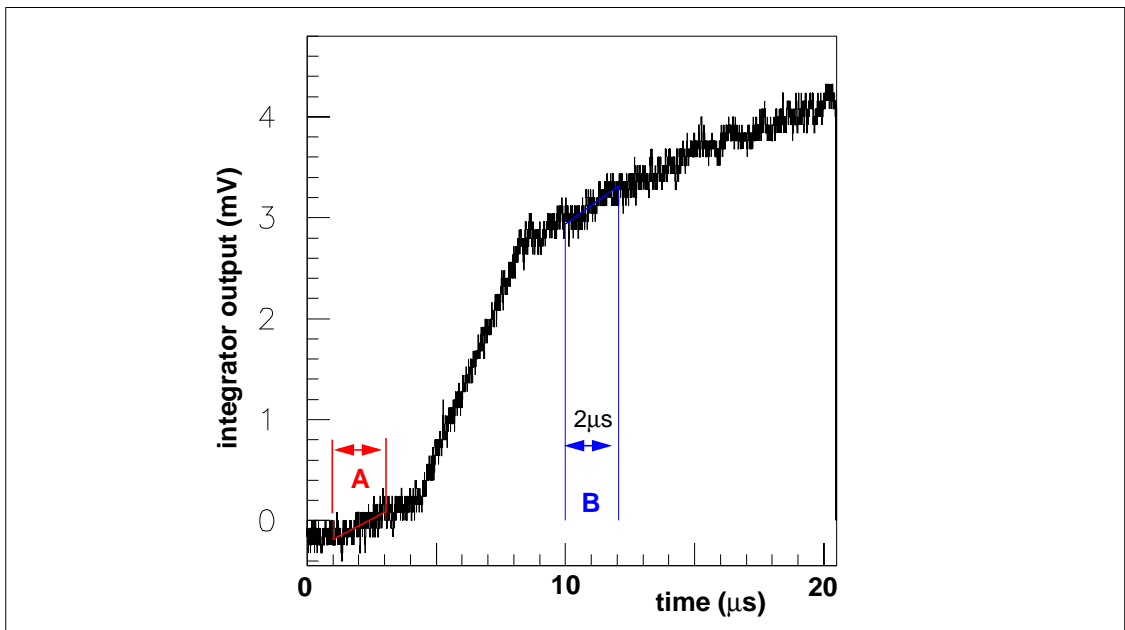

Figure 8: The signal measured at the output of the integrator is analysed in windows A and B as explained under Figure 5

The high frequency noise remains constant at a level of 10 nV/sqrt(hz), i.e. it yields, after after a 20 Mhz low-pass filter, a gaussian noise of 85 µV RMS.

The fluctuation of the difference of the mean signal in windows A and B ($\sigma(\bar{A} - \bar{B})/(\sqrt{2})$), contains all contributions from $1/f^{\alpha}$ noise.
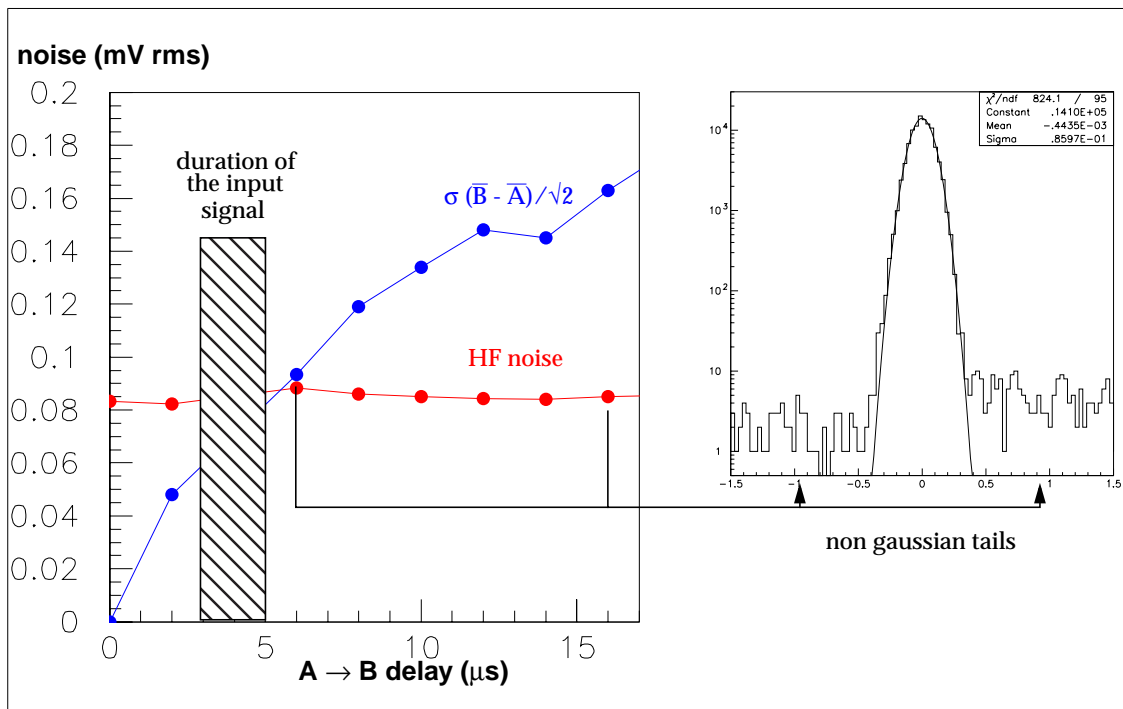
6

Figure 9: Summary of the main features of the integrator noise. Non-gaussian tails, due to glitches, are seen only in the bin following the input signal and the last one.

3.5 Problems

The following problems which appeared during the tests described above have been first solved empirically. They have not interfered much with the results presented so far.

3.5.1 baseline modulation problem

This effect is the cause of the polynomial subtraction developed in Section . The 20 µs time constant is transformed into 200 µs by decoupling the V_{ref} potential. Its maximum amplitude is about 110 mV as seen inFigure 10.
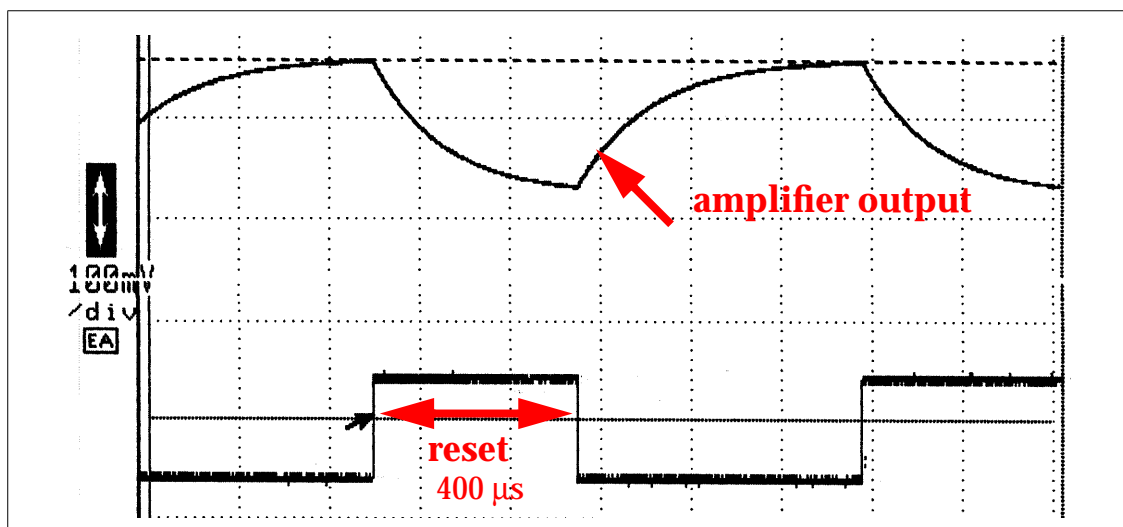

Figure 10: Baseline modulation by the reset in absence of input signal

3.5.2   amplifier transients

For a square signal input, some transients have been observed on both amplifier outputs. They are not symmetrical when changing the amplifier input or the polarity of the signal, as seen in Figure 11.
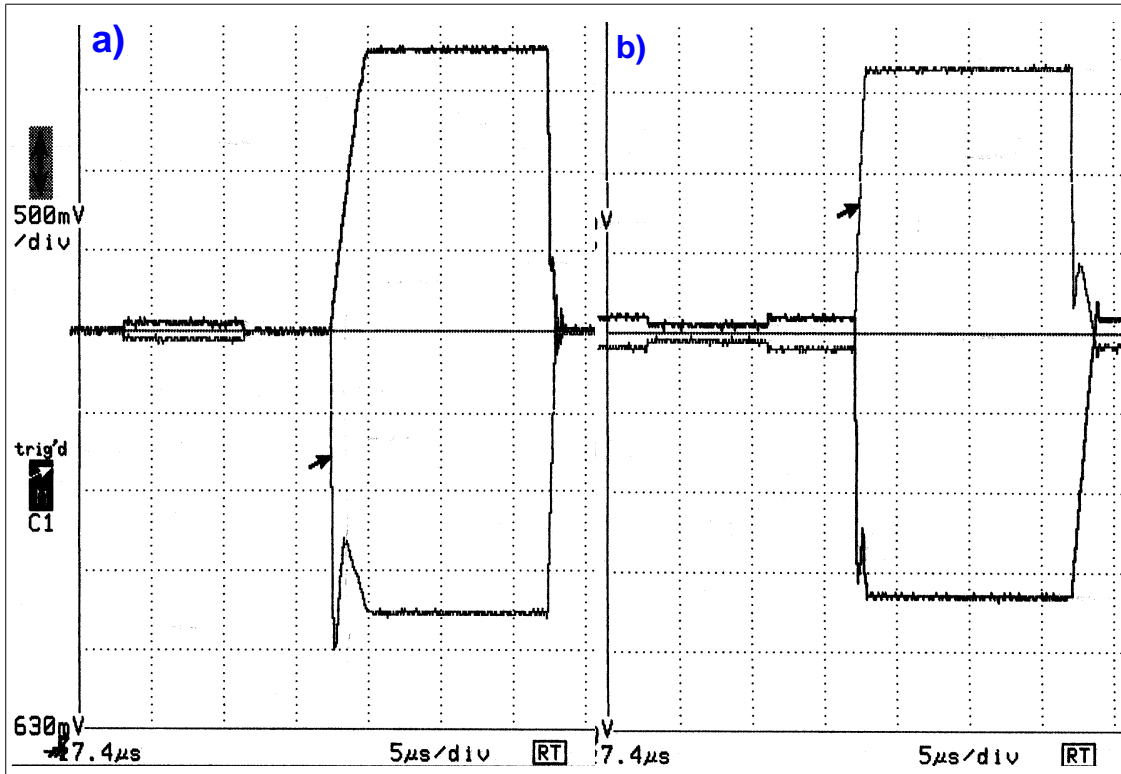

Figure 11:   Both amplifier outputs are figured for a square pulse fed on either entry of the amplifier (a or b). Transient are observed on either edge.

3.5.3   stability of the amplifier/integrator assembly

When the output of the amplifier is connected to the input of the integrator the system the system becomes unstable. This instability is cured by 330 pF capacitors connecting to ground both sides of the 2 resistors R_1, i.e. the 4 test points TP1 and TP2 (cf.Figure 1).

This trick has allowed a study of the complete system, as shown in Section 3.3, but it works only with the lower gain and not always.

4   Plans

4.1   Analytic approach

- simulate problems previously mentioned
- study of transients and timing constraints related to various switches, one clock at a time
- time constraints coming from the interaction between two clocks

4.2 System approach

- optimization of the timing diagram
- optimization of the gain chain
- completion of our complete chain (CCD -CDS -San Diego)
- comparison with alternate (simpler?) analog chains

Conclusion

- Electronic noise seems a factor x2 above simulation (itself a factor x2 above CCD output). If this hypothesis is verified, it leads to a waste of ADC range.
- Our CDS prototype is at the top of the complexity scale. It might be difficult to understand all the problems only by signal analysis joined to electronic simulation.
- It is necessary to integrate all these elements in order to design a realistic SNAP analog chain. In particular multiple gains would have a profound impact on this chain. A global perspective is important for us to focus tests on real issues.

Appendix 1: Tektronix DSA 602

As we use DSA 602 near its limits of speed and sensivity, we present an analysis of this instrument using the same tools than for CDS. Waveforms are recorded by 4 FADC with an 8 bit range. The sampling rate can be adjusted up to 2 ns per ADC. In our setup we use simultaneous recording of 2 waveforms with a 1Gsample per second -typically 10Ksample for our time windows of 10 μs. In this mode, 2 FADC are teamed for each channel. They are autocalibrated by the DSA, although not perfectly. The frequency spectrum of DSA input resulting from auto analysis is represented in Figure 12. (We understand the 250 Mhz line as the effect of mismatch between the two digitizer concurring to the record).
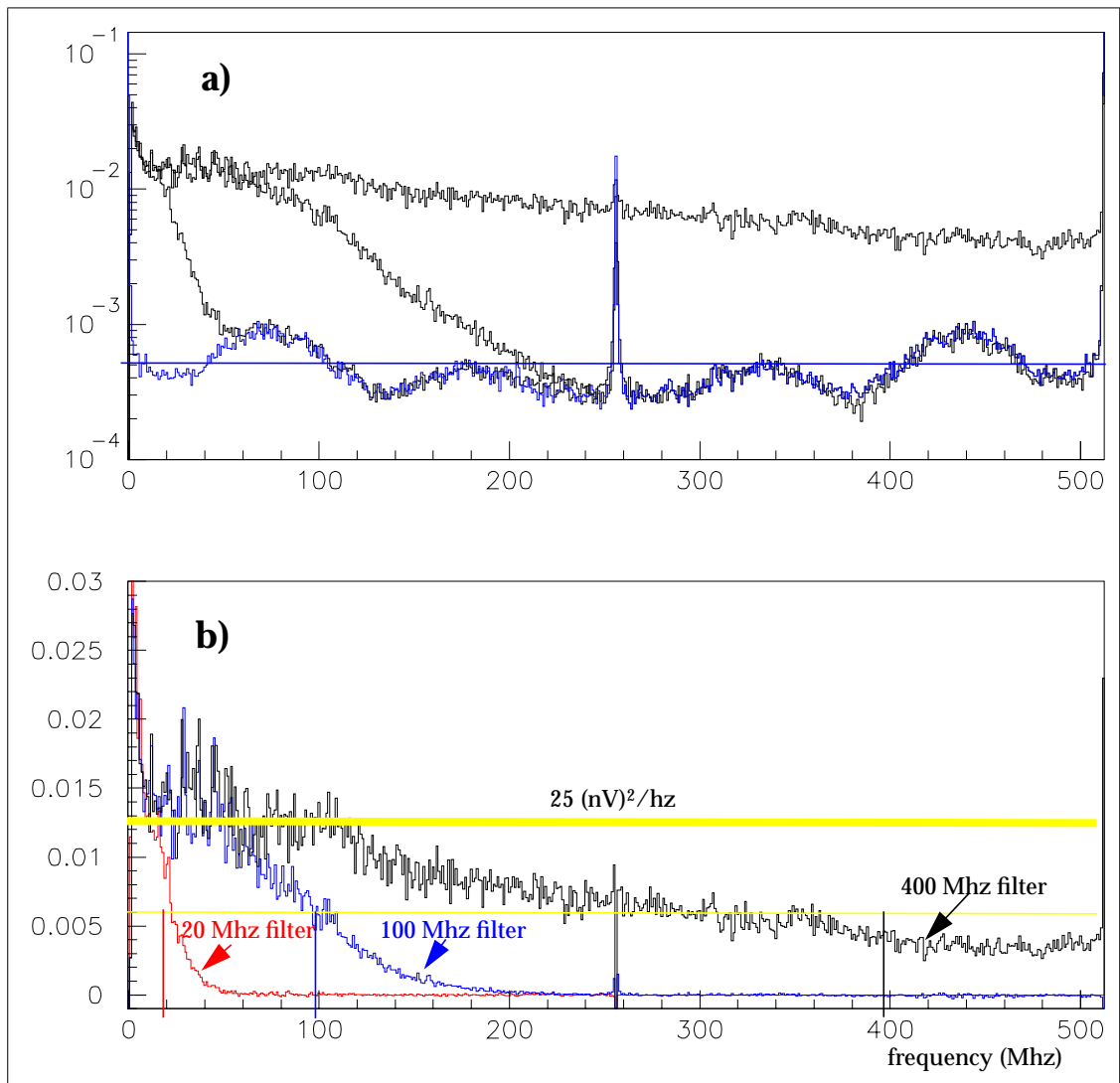

Figure 12: Power input spectrum of Digital Signal Analyser DSA 602 (noise power scale indicated by the $25 \, (nV)^2/hz$ line). a) with ADC quantization noise included, b) with quantization noise subtracted.t