Switched Capacitor Integrator Design and Simulations

Contents

Introduction

Switched capacitor integrators are main building blocks of switched capacitor filters and used in precise ADC structures. Analog filters build with resistors and capacitors require these components' values to be precise in order to maintain targeted frequency characteristics. On the other hand, switched capacitor filters only require capacitor ratios to be precise which is achieved by most of the processes. These properties make switched capacitor integrator valuable for most of the analog applications.

Analysis of the SC Integrator

Switched capacitor integrator circuit is shown in Fig. 1. This circuit is equivalent to the one shown in Fig.2 as switched capacitors are there to implement a resistor. The structure connected to the positive terminal of op-amp is the mirror of the switches and capacitors connected to the negative terminal of op-amp.It eliminates offset originating from charge injection of the switches. By determining a C_C value equivalent to capacitors at the negative terminal, charges injected at equal amounts at both sides with equivalent capacitor values generates equal volteges. Thus, op-amp is protected from charge injection distortion. To this end, C_C should be chosen as the sum of C_S, C_I and C_F, as C_C is functional only in the clock period when is 1, otherwise when Φ is 1 this node is set to reference voltage.

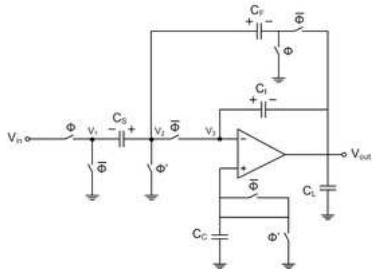

Figure 1 Switched Capacitor Integrator Circuit

It is convenient to analyze this basic circuit of Fig.2 at first, then to compare its results with the results of the circuit shown in Fig.1.

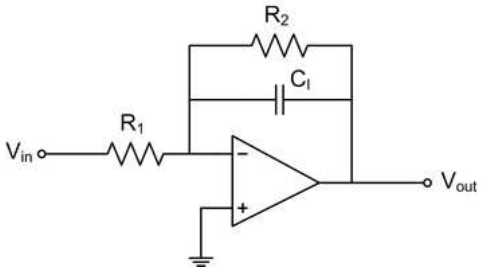

Figure 2 Simplified Integrator Structure

The op-amp is considered to be ideal, so there is no current between its terminals and voltages at its terminals are equal as the gain infinite. In this circuit terminals are at the ground, so current flowing through R_1 is V_{in}/R_1 and current flowing in the feedback is $(sC_I+1/R_1)V_{out}$. These currents should be equal as there is no current between terminals of op-amp. Relation between V_{in} and V_{out} can be revealed using this equation.

$$\frac{V_{in}}{R_1} = (sC_I + \frac{1}{R_2})V_{out}$$

$$\frac{V_{in}}{R_1} = (\frac{sC_I R_2 + 1}{R_2})V_{out}$$

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_1}.\frac{1}{sC_1R_2+1}$$

Values of the resistances and the capacitor should be chosen to provide a pole at 25 KHz and 2.5 gain. $s_p=2\pi f=2.\pi.25000=157080$ and for a 2.5 gain at low frequencies numerator of the transfer function should 2.5 times this pole value.

$$\frac{V_{out}}{V_{in}} = \frac{392700}{s+157080}$$

R_1,R_2 and C_1 values should be chosen to match this transfer function. We can convert this transfer function to discrete time using c2d command of Matlab,

$$\frac{V_{out}}{V_{in}} = \frac{0.674}{z-0.7304}$$

The transfer function that will be obtained later from the analysis of the circuit in Fig. 1 also match this transfer function.

To understand mechanism of the switched capacitor integrator, it is essential to understand where the input is sampled and where the output is set according to clock signals. Clock signals conducting the switches are shown in Fig.3. The segment where Φ and Φ' are 1, input is sampled. Here it is crucial that Φ' is closed before V_1 is grounded, so that sampled input is sampled properly. Otherwise, sampled value always is the reference voltage value. The segment where is 1, output is set. So, these clock signals should be non-overlapping to properly sample input values and setting correct outputs.

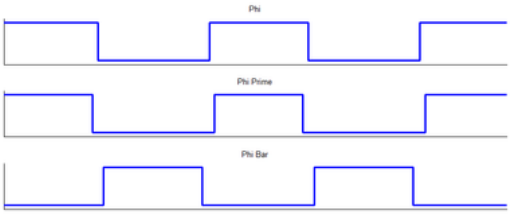

Figure 3 Clock Signals

As this evalution is realized with respect to clock signals, we should also conduct the analysis according to this clock signals. Let the segment where Φ and Φ' are 1 be t_1 and the segment where is 1 be t_2. During $t_1 \rightarrow t_2$, charge is conserved between positive terminals of capacitors and negative terminal of op-amp. Voltages at nodes during t_1 and t_2 are as follows:

$t_1 \rightarrow$ $V_1=V_{in}(t_1)$

$V_2=0$

$V_3=-1/K\,V_{out}(t_1)$

$V_{out}=V_{out}(t_1)$

$t_2 \rightarrow$ $V_1=0$

$V_2=-1/K\,V_{out}(t_2)$

$V_3=-1/K\,V_{out}(t_2)$

$V_{out}=V_{out}(t_2)$

Here, it is assumed that op-amp gain is K, not infinite, to obtain more realistic results. As voltages at terminals of capacitors are known, charges stored at capacitors can be calculated as Q=CV. Then, transfer function of the integtator can be found using charge conservation.

$$Q(t_1) = C_S[0-V_{in}(t_1)] + C_F(0-0) + C_I\left[-\frac{1}{K}V_{out}(t_1) - V_{out}(t_1)\right]$$

$$Q(t_2) = C_S\left[-\frac{1}{K}V_{out}(t_2) - 0\right] + C_F\left[-\frac{1}{K}V_{out}(t_2) - V_{out}(t_2)\right] + C_I\left[-\frac{1}{K}V_{out}(t_2) - V_{out}(t_2)\right]$$

$$\Rightarrow Q(t_1) = Q(t_2)$$

$$-C_S V_{in}(t_1) - C_I.\frac{K+1}{K}.V_{out}(t_1) = -\left[C_S.\frac{1}{K} + (C_F+C_I).\frac{K+1}{K}\right].V_{out}(t_2)$$

$$KC_S V_{in}(t_1) + (K+1)C_I V_{out}(t_1)$$

$$= [C_S + (K+1)(C_F + C_I)].V_{out}(t_2)$$

Setting $V_{out}(t_2)=V_{out}(z)$ and $V_{in}(t_1)=z^{-1}.V_{in}(z)$, $V_{out}(t_1)=z^{-1}.V_{out}(z)$ in the equation,

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{KC_S}{[C_S + (K+1)(C_F + C_I)].z - (K+1)C_I}$$

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{\frac{KC_S}{[C_S+(K+1)(C_F+C_I)]}}{z - \frac{(K+1)C_I}{[C_S+(K+1)(C_F+C_I)]}}$$

If we assume that op-amp gain is much higher than other parameters, we can further simplify the equation as follows:

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{\frac{C_S}{C_F+C_I}}{z - \frac{C_I}{C_F+C_I}}$$

Pole frequency of the integrator should be 25 kHz. $C_I/(C_F+C_I)$ ratio is set to provide this pole frequency. As $z=e^{sT}$,

$$\frac{C_I}{C_F + C_I} = e^{-2\pi.25K.\frac{1}{500K}} \cong 0.7304$$

Integrator gain should be 2.5 . To find $C_S/(C_F+C_I)$ ratio providing this gain, z is set to 1, while $C_I/(C_F+C_I)$ =0.7304 in the transfer function, then result is as follows:

$$\left.\frac{\frac{C_s}{C_F+C_I}}{z - 0.7304}\right|_{z=1} = 2.5$$

$$\frac{C_s}{C_F + C_I} \cong 0.674$$

Eventually, the ideal transfer function is found to be

$$\frac{V_{out}}{V_{in}} = \frac{0.674}{z - 0.7304}$$

which is exactly the same as the one found for basic integrator circuit. From above values, we can obtain capacitor ratios $C_S/C_F=2.5$ and $C_I/C_S=1.0837$.

Magnitude and phase of the transfer function can be plotted using *bode* command of Matlab as shown in Fig.4.

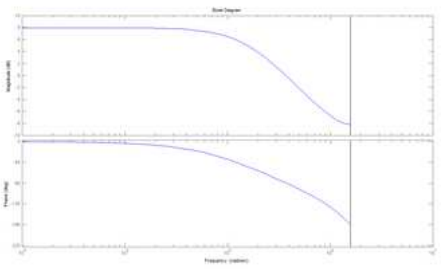

Figure 4 Bode plot of the ideal transfer function

In the above plot, a 8dB gain and a pole frequency at 1.57 10^5 rad is observed. 8dB is equivalent to 2.5 and 1.57 10^5 rad is equal to 25 KHz. As the sampling frequency is 500 KHZ, values at frequencies higher than 250 KHz are not shown and there is a black line indicating this frequency in the plot.

Clock Generation

As it was stated before, switched capacitor integrator circuits are in need of non overlapping clocks. To make sure a proper sampling is achieved, another clock with different fall timing is needed. These clocks are defined as phi, phi prime and phi bar in Fig. 3. For the generation of these clocks from a single Vpulse, clock generation circuit is designed. It can be seen in Fig. 5. As design inputs, only supply, ground and Vpulse voltages are used. Waveforms of the clock signals generated by this curcuit are shown in Fig. 6. Since, resolution is not enough to see transitions of the signals and the non-overlapping characteristics of the clock, Fig. 7 and Fig. 8 is created to show waveforms zoomed to falling and rising edges of phi in given order.

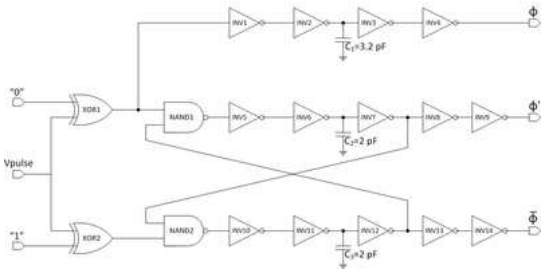

Figure 5 Schematic of clock generation circuit.

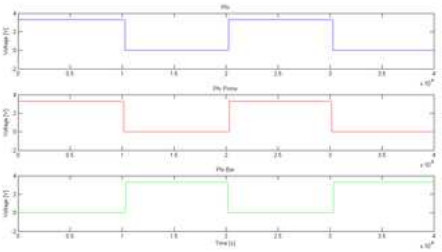

Figure 6 Waveforms of phi, phi prime and phi bar.

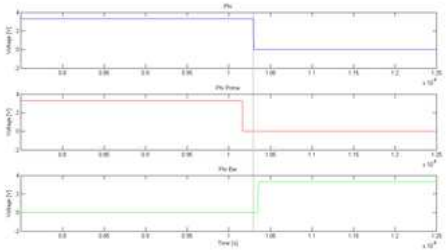

Figure 7 Waveforms of phi, phi prime and phi bar. (Zoomed to falling edge of phi.)

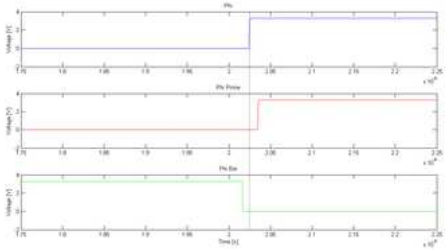

Figure 8 Waveforms of phi, phi prime and phi bar. (Zoomed to rising edge of phi.)

Design of Operational Amplifier

An OPAMP with 103.3 dB DC gain, 10.53 MHz of GBW and 60.60 phase margin is designed to be used in switched capacitor integrator. Schematic of OPAMP is shown in Fig. 9.

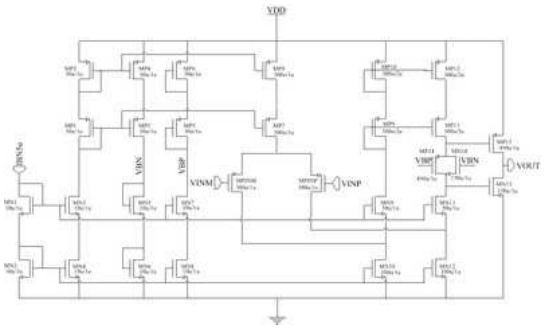

Figure 9 Schematic of op-amp.

AC simulation schematic and results for gain, phase can be seen in Fig. 10 and Fig. 11 respectively.

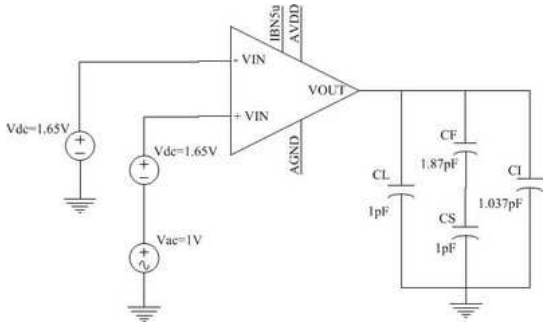

Figure 10 Simulation setup for the test of op-amp.

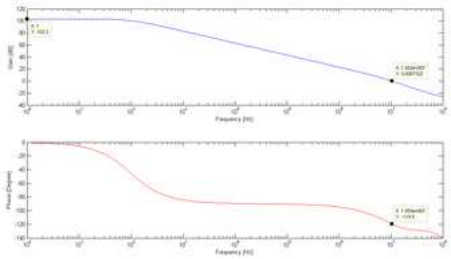

Figure 11 Gain and phase characteristic of op-amp.

Switches

In our design transmission gates are used for switching purposes. Using transmission gates, we can supply an output range 0 - 3.3 V. Using only a NMOS or PMOS causes the integrator to be unbalanced. In the case of using a single NMOS as a switch, output has an equilibrium point above 1.65 V and inputs above 1.65 V are amplified more than targeted gain value. These imperfections are experienced during early stages of our project. Transistor sizes are chosen with respect to the trade-off between low Ron resistance with large W/L ratios and charge injection effect caused by the same large W/L ratios. Transistor lengths are chosen to be 0.35 μm and transistor widths are 10 μm, 20 μm for NMOS and PMOS respectively.

Simulation Results

PAC Simulation

PAC gain and phase of the circuit are plotted on Fig. 12 with z-domain transfer function Bode results. For a better interpretation of the differences between these plots, PAC results are also plotted against s-domain transfer function Bode results. Blue line displays results for PAC simulation, red line for Bode results.

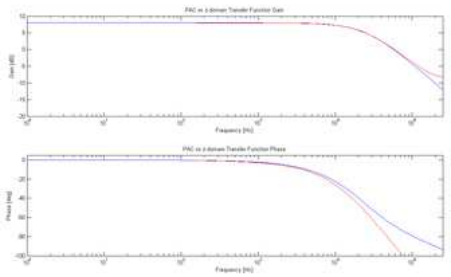

Figure 12 PAC results with z-domain transfer function Bode results

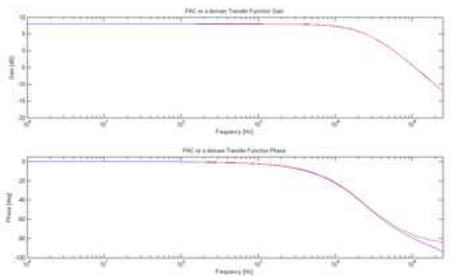

Figure 13 PAC results with s-domain transfer function Bode results

PAC results better match s-domain transfer function Bode results. A transfer function with a single pole in left half plane, shows a 20 dB/decade decline and 90^0 phase shift around pole frequency. PAC results provides these characteristics and matches good with s-domain Bode results. A possible reason of this defect is that Bode algorithm does not work properly for frequencies close to Nyquist frequency.

PAC simulation is also used for measuring PSRR. Fig. 14 shows results for PSRR measurements.

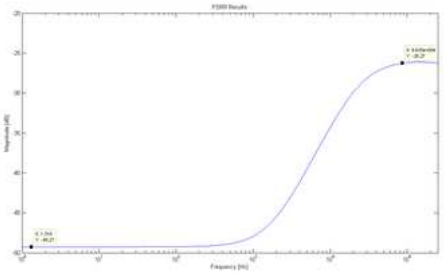

Figure 14 PSRR Results

As it can be seen seen from the figure PSRR is -49 dB for low frequencies, it falls to -26 dB for high frequencies.

Simulation of Integrator Linearity

Linearity of integrator is measured with Vsin sources at 5 different frequencies, 5 KHz, 10 KHz, 15 Khz, 20 KHz, 25 KHz and 1V peak to peak amplitude. Output is observed by transient analysis and it is followed by DFT of output transient. Fig. 15, Fig. 16, Fig. 17, Fig. 18 and Fig. 19 show DFTs of output transients with Vsin source frequencies at 5 KHz, 10 KHz, 15 Khz, 20 KHz and 25 KHz respectively.

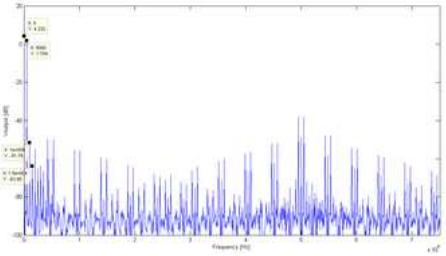

Figure 15 DFT of output voltage with Vsin source frequency at 5 KHz.

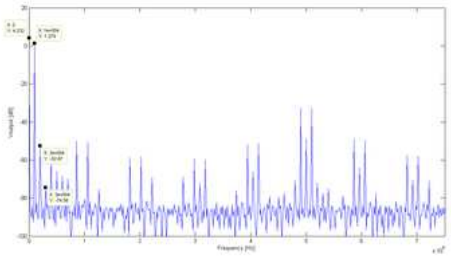

Figure 16 DFT of output voltage with Vsin source frequency at 10 KHz.

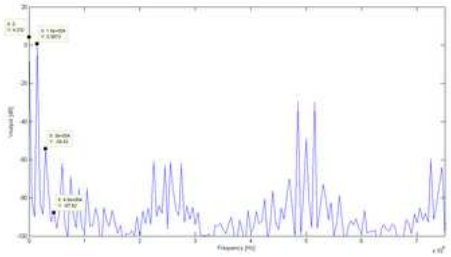

Figure 17 DFT of output voltage with Vsin source frequency at 15 KHz.

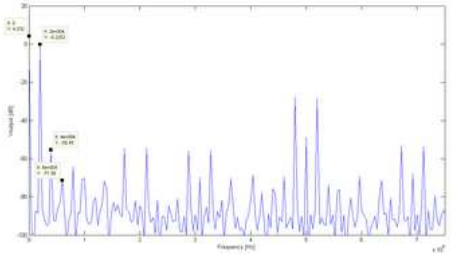

Figure 18 DFT of output voltage with Vsin source frequency at 20 KHz.

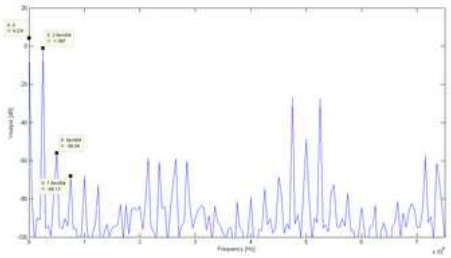

Figure 19 DFT of output voltage with Vsin source frequency at 25 KHz.

As it can be seen from figures above, second, third and other harmonics oriented by Vsin source are rather low. However, there is another harmonic that can be considered as high. It is oriented from 500 KHz, with sinc(x) like characteristic. Since, observed output sinus function sampled by 500 KHz clock, harmonics in that frequency is expected. Also, as frequency gets higher, number of sampling that occur in a period decreases. Therefore, it is expected that harmonics at 500 KHz increase as source frequency increases. It should also be stated that many of related harmonics are not in our primary frequency spectrum which is Fs/2 (250 KHz), so they can be disregarded.

PNOISE Simulation for Integrated Noise

PNOISE simulation is run for the circuit selecting timedomain option from noise type section. 15 points have been examined in 2 µs range as the clock frequency is 500 KHz. Reference sideband is selected to be zero as we are interested in 10 Hz to 10 KHz frequency range and according to equation $|f_{in}| = |refsideband*f_{PSS} + f_{out}|$ [1]. Noise spectrums at the output for these 15 points are shown in Fig. 20 for 10 Hz to 10 KHz range. Integrated noise from 10 Hz to 10 KHz for these 15 points are shown in Fig. 21.

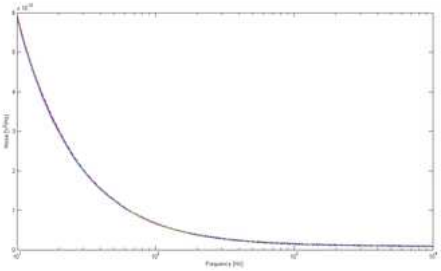

Figure 20 Noise Spectrum of Test Points

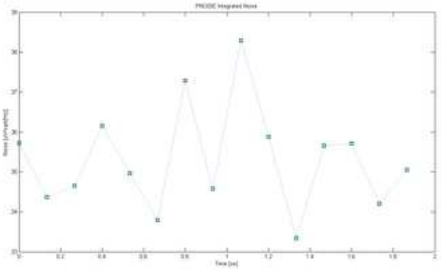

Figure 21 Integrated Noise of Test Points

As we can see from noise spectrum, noise level decreases with frequency. This indicates that dominant noise contributor is flicker noise (1/f noise). The flicker noise power in MOSFET can be expressed as follows [2],

$$\overline{V_n^2} = \frac{K}{C_{ox} WL} \cdot \frac{1}{f}$$

which states that flicker noise can be reduced using smaller transistors. This equation also indicates that this flicker noise mainly originates from operational amplifier as transistors with relatively large W/L ratios are employed within the op-amp. Another solution to reduce flicker noise is to reduce DC current, or to prefer PMOS as it employs holes not electrons [2]. Thermal noise and shot noise is negligible at this frequency range. Burst noise is expected to be around 500 KHz. Clock jitter is also another important noise contributor.

Conclusion

Simulation results indicate that designed switched capacitor integrator works properly. Its frequency characteristics are as expected. PSRR value is acceptable and noise level is low. Enhancements that would be useful are making use of a better op-amp, using better designed switches which can compensate charger injection effects, protection from power supply noise. Measurements improving integrator linearity should be taken for an integrator of good quality.

References

[1] Retrieved from “http://www.designers-guide.org/Forum/YaBB.pl?num=1038418160”, on January 23th, 2011
[2] B. Razavi, Design of Analog CMOS Integrated Circuits, Mc Graw Hill Education, 2001.