Correlated Double Sampling in Capacitive Position Sensing Circuits for Micromachined Applications

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Abstract

In micromachined applications, the size of the sense capacitance is typically limited by the technology to a few hundreds femtofarads, thus resulting in a large sampling (kT/C) noise. This paper demonstrates that correlated double sampling (CDS), which has traditionally been used to remove the amplifier offset and attenuate the 1/f noise, can be extended to cancel the kT/C noise and the switch charge injection due to switching operations. A 4dB noise reduction in the prototype sensing circuit confirms this concept. By optimizing the thermal noise of the amplifier, analytical results show that the kT/C noise cancellation can reduce the thermal noise of the sensing circuit by as much as 20dB.

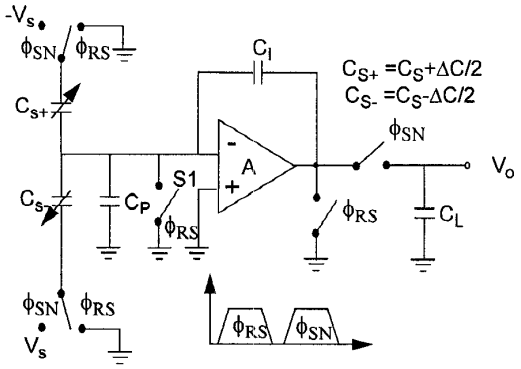

Fig. 1: A typical switched-capacitor capacitance sensing circuit

1. Introduction

Variable capacitors serve as the interface in various micromachined systems, such as accelerometers, rate gyroscopes, pressure sensors, and microactuators. These capacitors generally can be approximated as parallel-plate capacitors, in which the overlapping area of the plates or the spacing between the plates is a function of the displacement of the sense element. Fig. 1 shows a typical switched-capacitor capacitance measurement circuit. The output voltage of this circuit is

$$v_o = \frac{\Delta C}{C_I} \cdot V_S \,. \qquad \text{(Eq 1)}$$

Because of the technology-imposed size restriction on the sense element, the sense capacitance C_S and the capacitance variation ΔC are very small, normally in the range of hundreds of femtofarads and 1-100 attofarads (atto=10^{-18}), respectively. With an integrating capacitance C_I roughly the same size as the sense capacitance, the output voltage is in the order of 10μV to 1mV. To achieve a high resolution, a low-noise low-offset capacitance-sensing scheme is required. This paper demonstrates that Correlated Double Sampling (CDS), which is normally used to cancel amplifier offset and flicker noise, can be extended to cancel kT/C noise and switch-charge injection.

2. Correlated Double Sampling Technique

Correlated double sampling can be implemented to the circuit shown in Fig. 1 by simply

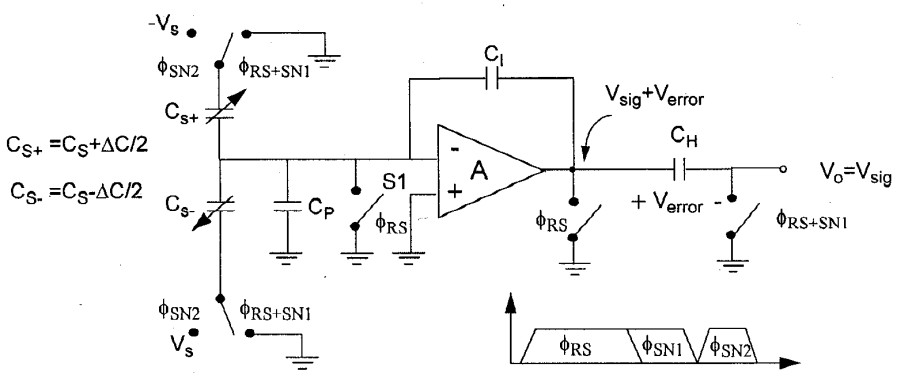

Fig. 2: This circuit is modified from the one in Fig. 1 to perform correlated double sampling by adding an error storage capacitor C_H and another sensing phase.

adding an error-storage capacitor C_H and an additional clock phase, as illustrated in Fig. 2. The operations of this circuit can be explained as follows. At the end of the reset phase, the sampling switch S_1 is opened, thus injecting charge and kT/C noise into the amplifier summing node. During the error sensing phase ϕ_{SN1}, the error which consists of the amplifier offset and 1/f noise, charge injection, and kT/C noise is amplified and stored on capacitor C_H. During the signal sensing phase ϕ_{SN2}, the sense voltages $(\pm V_S)$ are applied to the sense capacitors. The amplifier output which contains both the signal and the error is subtracted by the error previously stored on C_H; therefore, the output voltage v_o contains only the signal. To the first order, the amplifier offset, switched-charge injection and kT/C noise are completely cancelled, while the 1/f noise is strongly attenuated at low frequencies by the noise shaping function of correlated double sampling [1].

With the kT/C noise and other errors removed, the amplifier thermal noise becomes the dominating noise source; hence, it needs to be minimized. The output-referred noise of the amplifier in Fig. 2 is

$$\frac{\overline{v_{opamp}^2}}{\Delta f} = \left(\frac{C_S + C_I + C_P + C_{GS}}{C_I}\right)^2 \cdot \frac{\overline{v_n^2}}{\Delta f} \quad \text{(Eq 2)}$$

where $\overline{v_n^2}$ is the input-referred noise of the amplifier and C_{GS} is the gate capacitance of the amplifier input device. In a properly designed amplifier, the input transistors are the dominant noise contributors. The thermal noise of a MOS transistor can be reduced by increasing the transconductance g_m. Increasing g_m, however, requires increasing either the saturation voltage of the input devices, which in practice is limited by the supply voltage, or enlarging the device size. This, in turn, increases the gate capacitance C_{GS} and the output-referred noise given in Eq. 2. The minimum amplifier noise, for a given saturation voltage, can be calculated as follows.

Substituting the input-referred thermal noise of the amplifier

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{16kT}{3g_m} \quad \text{(Eq 3)}$$

(assuming that the input devices are the dominant noise contributors) and the cutoff frequency relationship

$$f_T = \frac{g_m}{2\pi C_{GS}} \quad \text{(Eq 4)}$$

into Eq. 2 yields

$$\frac{\overline{v_{opamp}^2}}{\Delta f} = \frac{(C_S + C_I + C_P + C_{GS})^2}{C_{GS}C_I^2}\frac{8kTn_f}{3\pi f_T}. \quad \text{(Eq 5)}$$

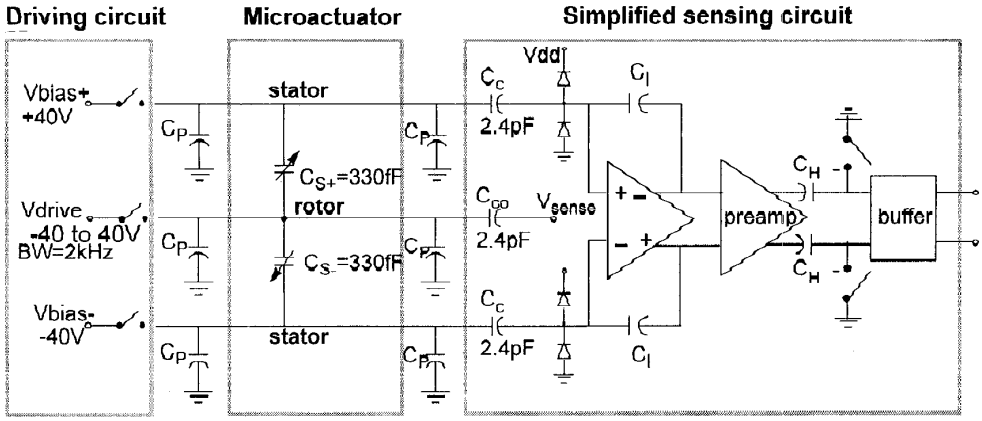

Fig. 3: Simplified circuit diagram of the capacitive position sensing interface. All the switches in the sensing circuit, except the CDS switches, are omitted for simplicity.

Next, differentiate Eq. 5 with respect to C_{GS} results in the optimal input device size,

$$C_{GS} = C_S + C_I + C_P \ . \qquad \text{(Eq 6)}$$

Substituting Eq. 6 into Eq. 5 yields

$$\frac{\overline{v_{opamp}^2}}{\Delta f} = \frac{(C_S + C_I + C_P)}{C_I^2} \cdot \frac{32kT}{3\pi f_T} . \qquad \text{(Eq 7)}$$

Taking into account the amplifier noise folding and the double sampling, and assuming a 25% duty cycle for each sensing phase [3],

$$\frac{\overline{v_{opamp}^2}}{\Delta f} = \frac{(C_S + C_I + C_P)}{C_I^2} \cdot \frac{64 n_\tau kT}{3\pi f_T} \qquad \text{(Eq 8)}$$

where n_τ is the number of settling time constants and is typically in the range of seven to ten.

In comparison, the output-referred kT/C noise, which is normally the dominant noise source in a circuit without correlated double sampling, is

$$\frac{\overline{v_{kT/C}^2}}{\Delta f} = \frac{1}{f_s} \cdot \left(\frac{C_S + C_I + C_P + C_{GS}}{C_I}\right)^2 \cdot \left(\frac{kT}{C_S + C_I + C_P + C_{GS}}\right) \qquad \text{(Eq 9)}$$

where f_s is the sampling frequency of the circuit. From Eq. 6 and Eq. 7, the noise improvement due to correlated double sampling can be calculated as

$$\text{Noise improvement} \approx \frac{3\pi f_T}{16 n_\tau f_s} \propto \frac{f_T}{f_s} \qquad \text{(Eq 10)}$$

Due to the low bandwidth of most micromachined applications, the sampling frequency f_s can be thousands of times smaller than the cutoff frequency f_T; therefore, the noise improvement can be as large as 20dB. In practice, power consumption often limits the use of optimally sized input devices in the amplifier and the noise improvement is reduced to the order 10dB.

3. An experimental system and measurement results

Correlated double sampling was implemented in a capacitive position sensing circuit for microactuators [4], as a part of a dual-stage servo system for magnetic disk drives [5]. Fig. 3 shows the simplified circuit diagram of the position sensing circuit, the driving circuit, and the microactuator. In this sensing circuit, correlated double sampling is performed at the preamplifier output; hence, the errors from both the front-end amplifier and the preamplifier are cancelled. On-chip coupling capacitors (C_c) are used to shield the sensing electronics from the high voltage drive of the microactuator, thus allowing the

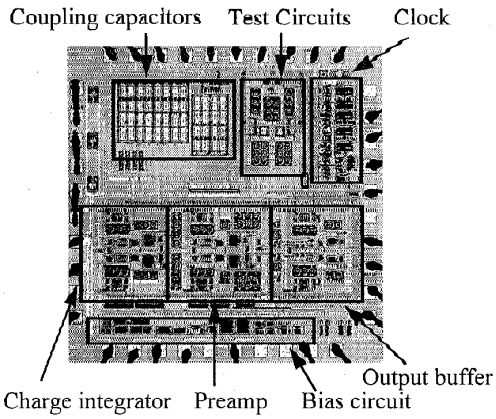

Fig. 4: Die photograph of the position sensing circuit fabricated in a 1.2-μm 5V CMOS. The die area is 2.2*2.2 mm^2.

sensing electronics to be fabricated in a conventional CMOS process. Furthermore, time and frequency division allow the sensing and the driving to share a single set of actuator electrodes. The sensing electronics was fabricated in a 1.2-μm 5-volt CMOS process with the die photograph shown in Fig. 4.

The measured offset and 1/f noise corner of the sensing electronics are 10mV and 100Hz, respectively, contributed mainly by the output buffer. Without the correlated double sampling, the offset and the 1/f noise corner will be determined by the front-end amplifier and can be as high as 300mV and 1MHz, respectively.

This prototype confirms the kT/C noise cancellation by correlated double sampling. The measured thermal noise of 700 $nV/\sqrt{Hz}$ is 4dB lower than the calculated combined kT/C and amplifier thermal noise of 1140 $nV/\sqrt{Hz}$. In this prototype, the noise improvement is rather small because the power consumption and the die area constraints of this application exclude the use of an amplifier with lower thermal noise.

5. Conclusions

Correlated double sampling can remove the amplifier offset and 1/f noise, charge injection, and kT/C noise due to switching operations in capacitive position sensing circuits. The prototype circuit demonstrates a noise improvement of 4dB due to the cancellation of kT/C noise. By optimizing the amplifier thermal noise, analytical results show that a noise improvement of 10 to 20dB is achievable.

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