Fabrication of microshutter arrays for space application

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Abstract

Two-dimensional microshutter arrays are being developed at NASA Goddard Space Flight Center for the Next Generation Space Telescope (NGST) for use in the near-infrared region. Functioning as object selection devices, the microshutter arrays are designed for the transmission of light with high efficiency and high contrast. The NGST environment requires cryogenic operation at 45K. Arrays are close-packed silicon nitride membranes with a pixel size of 100 X 100 micrometers . Individual shutters are patterned with a torsion flexure permitting shutters to open 90 degrees with a minimized mechanical stress concentration. The mechanical shutter arrays are fabricated with MEMS technologies. The processing includes a RIE front-etch to form shutters out of the nitride membrane, an anisotropic back-etch for wafer thinning, and a deep RIE (DRIE) back-etch down to the nitride shutter membrane to form frames and to relieve shutters from the silicon substrate. Two approaches for shutter actuation have been developed. Shutters are actuated using either a combined mechanical and electrostatic force or a combined magnetic and electrostatic force. A CMOS circuit embedded in the frame between shutters allows programmable shutter selection for the first approach. A control of row and column electrodes fulfills shutter selection for the second approach.

Fabrication of Microshutter Arrays for Space Application

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Abstract

Two-dimensional microshutter arrays are being developed at NASA Goddard Space Flight Center for the Next Generation Space Telescope (NGST) for use in the near-infrared region. Functioning as object selection devices, t microshutter arrays are designed for the transmission of light with high efficiency and high contrast. The NGST environment requires cryogenic operation at 45K. Arrays are close-packed silicon nitride membranes with a pixel size of 100x100 µm. Individual shutters are patterned with a torsion flexure permitting shutters to open 90 degrees with a minimized mechanical stress concentration. The mechanical shutter arrays are fabricated with MEMS technologies. The processing includes a RIE front-etch to form shutters out of the nitride membrane, an anisotropi back-etch for wafer thinning, and a deep RIE (DRIE) back-etch down to the nitride shutter membrane to form frames and to relieve shutters from the silicon substrate. Two approaches for shutter actuation have been develope Shutters are actuated using either a combined mechanical and electrostatic force or a combined magnetic and electrostatic force. A CMOS circuit embedded in the frame between shutters allows programmable shutter selecti for the first approach. A control of row and column electrodes fulfills shutter selection for the second approach.

Key Words: microshutter, MEMS, DRIE, micro-optics, near-infrared

1. Introduction

selector is needed for the MOS in order to prevent spectral overlap. The primary requirements for the selec include: a 2000 x 2000 array with a 100μm pixel size to cover the large NGST field of view; a fill factor, i.e. t total selecting element area over total selector array area, of 80% or better; and an operation in a cryoge temperature range around 45K to assure negligible thermal emission of the instrument.

Micromirror array technology developed by Texas Instruments has been a major candidate for use to make t object selector for the MOS on NGST[2,3]. The advantage of developing micromirror arrays has to be the use o mature technology in the development of devices with large array and small pixel sizes. Micromirror arrays m also provide a high fill factor because all actuation/addressing circuits can be hidden underneath the mirr elements. The disadvantage using a micromirror array as an object selector is that micromirrors are reflecti devices. They diffract and scatter light and therefore provide lower contrast. An alternative approach to micromir array devices is to develop microshutter array devices for the MOS application. Microshutters are transmiss because they can be fully open so to allow light going through. Microshutter devices have the potential to achie higher contrast than reflective devices. Besides the NGST application, microshutter arrays also have potential in u for laser filtering and mass-spectroscopy, etc.

Moseley et. al. have designed and been developing microshutter arrays with addressable actuation functions[4]. T proposed shutter array design consists of a 2048x2048 array as a mosaic of 16 512x512 arrays of transmiss shutters with a fill factor of 80%. Each shutter covers an area of 100x100μm and is connected to a frame throug neck region and a torsion beam, as shown in Figure 1. Shutters open 90 degree out of plane through a shutter along the axis of the torsion beam combined with a torsion of the beams. In previous work, material selection

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shutters was carried out through a series of mechanical testing and numerical analysis[5,6]. Mechanical responses torsion beams were studied to optimize their physical sizes and geometry[6]. Shutter array actuation mechanisms w developed and prototypic devices were practiced towards the goal of programmable addressing and fill-fac maximizing [6,7].

Figure 1. SEM image of a microshutter (left) and a shutter opened using a probe (right)

This work is focused on the fabrication of microshutter arrays. In the fabrication, the challenges are from t aspects: mechanical shutter array fabrication and addressable shutter array actuation. The key measure in the asp of mechanical shutter array fabrication is the capability to make shutters with large array sizes. The requirement o less. We have developed fabrication techniques to integrate two addressable actuation mechanisms, respectively mechanical shutter array fabrication. They are the double shutter mechanism with mechanical and electrosta actuation, and the single shutter mechanism with magnetic and electrostatic actuation. We are working towards t fabrication of 512x512 arrays with a frame width of 2µm. Serving MEMS technologies developed in recent yea deep reactive ion etching (DRIE) is a powerful tool and a critical step in the fabrication of microshutter arrays. this paper, the application of DRIE and especially the control of DRIE parameters are addressed and discussed.

2. Fabrication of Microshutter Arrays

Microshutter array fabrication is carried out through conventional semiconductor processing and MEMS techniqu developed in recent years. Mechanical shutter array fabrication is developed based on the bulk MEMS technolo which will be described in Section 2.1. Between the two options for actuation designs as introduced earlier, t double-shutter design, requires mechanical actuation and electrostatic holding. CMOS fabrication has be integrated in the mechanical shutter array processing for shutter addressing. The detail will be presented in Secti 2.2. The single-shutter array design requires magnetic actuation and electrostatic holding. The fabrication of the functional elements has also been integrated in mechanical shutter array processing and will be described in secti 2.3. DRIE is a critical processing step in the fabrication of microshutter arrays. The control of DRIE processing w be discussed in these sections based on the mechanical shutter array design and the actuation mechanisms.

2.1 Mechanical Shutter Arrays

Four-inch single-side polished silicon wafers in thickness of 300µm, 400µm and 500µm have been used to ma microshutter arrays. The processing procedures for the fabrication of mechanical shutter arrays are shown in figu 2. A layer of 250nm thick low-temperature silicon oxide (LTO) or thermal oxide is first grown on the silic substrate as etch stops. A layer of low-stress silicon nitride is deposited on the silicon oxide using low-pressu chemical vapor deposition (LPCVD). The 500nm-thick silicon nitride is the actual material for microshutter blad We tested the silicon nitride wafers from three sources for this application. Microshutter arrays are patterned on t

front side of wafers with positive photoresist Shipley 1811 (see figure 3(a)). There are six 128x128 shutter arra ten 32x32 arrays, and a number of 8x8 arrays, as well as other test structures on the wafer. The total area combini all these shutter arrays and all test structures in the wafer is equivalent to the area of a 512x512 shutter array. T individual microshutters are in 100µm pixel size as shown in figure 1. We designed shutter arrays in the variation torsion beam widths and shutter frame widths. After a UV-exposure and the development in Shipley MF-3 developer, the patterned silicon nitride on the front side of the wafer is etched using a reactive ion etching (R (MARCH CS-1701) to form microshutters. The wafer is then flipped over and attached on a quartz carrier wa with a very thin layer of wax (10~15µm). Quartz wafers provide possibilities of back-alignment and the ease wafer handling when shutter frame is thinned down in later processing steps. Silicon nitride and silicon oxide on t back side of the wafer are etched off using a RIE and a buffered hydrofluoric acid (BHF) etching, respective Silicon exposed on wafer backside is etched in potassium hydroxide (KOH) at an elevated temperature, 65°C in t next step, wafer thinning. The wafer thickness is reduced from the starting thickness of 300µm, 400µm, and 500 to the desired 100µm. The second back etch is conducted through DRIE (STS Multiplex ICP System) to fr shutters from silicon substrate. Shutter array windows are patterned on the back of wafers with a thick positi photoresist (Shipley SJR 5740). The patterned photoresist is used as the mask for the DRIE etching and its thickn is in a range of 5~6µm in order to survive DRIE etching.

Backside Nitride and Oxide Layers

Shutter and torsion strap design etched into nitride with RIE.

Remove silicon from behind shutter by DRIE.

Quartz wafer attached to shutter wafer with transparent wax.

Remove oxide with HF

Shutter wafer etched in KOH down to buried oxide.

Buried oxide patterned as DRIE mask for the array frame.

Release array from quartz wafer

Figure 2. Fabrication procedures for mechanical shutter arrays

The DRIE etching is conducted through the Bosch process. The primary control of silicon etching in the Bos process is achieved by performing passivation and etching cycles, alternatively. In a passivation cycle, CF_n polyn from a C_4F_8 plasma, is deposited on all surfaces. In an etch cycle, polymer is removed from the base at much higl rate than from side-walls. Fluorine species from SF_6 plasma then etch exposed silicon surfaces. The process relies a number of processing parameters, such as RF coil power, platen substrate power, gas flow, pressure, depositi time, deposition/etch switching time, wafer size, etch pattern design, and exposed silicon area. These parameters a quite related regarding their effects on the silicon etch. Optimizing of these parameters requires practices accordi to requirements of the work, such as etch profile, aspect ratio, selectivity, etch rate, uniformity, undercut contr notching control, et. al.. The etch profile gives the profile of side walls out of the deep etching. The aspect ra presents the ratio of the etching depth over the size of window to be etched. The selectivity is the ratio of etch ra of silicon versus etch-stop mask materials, in our case, silicon versus photoresist. The etch rate is the rate for silic etch. The uniformity is defined as the etch-rate difference from etching area to etching area within a wafer. T undercut gives the profile of silicon over-etching underneath the etch-stop mask layer. The notching, on the otl hand, is the profile of silicon over-etching right above etch-stop membranes in the end of deep etching. In the ca

of microshutter arrays for NGST application, the etch profile, the uniformity, and the notching control are mo critical than other aspects. They will be discussed in next two sections. Figure 3(b) shows a shutter wafer after DF etching. One can see through the shutter arrays where only 500nm silicon nitride membranes and shutter fram remain.

(a) (b)

Figure 3. Microshutter arrays and test structures are shown on a four-inch wafer. There are six 128x128 shutter arrays, ten 32x arrays, and a number of 8x8 arrays, as well as other test structures on the wafer. The total area combining all shutter arrays a all test structures in the wafer is equivalent to the area of a 512x512 shutter array. (a) before DRIE etching, and (b) after DF etching.

After DRIE etching, the shutter wafer together with the carrier wafer goes again through a BHF etch to remove t etch-stop silicon oxide. The final step for mechanical microshutter array processing is the separation between shut device wafer and carrier wafer through a solvent soaking. Microshutter arrays are finally free from the carrier wa and individual microshutters are suspended through the only connection, the torsion beams, to shutter frames. V put effort on fabricating microshutter arrays with narrow torsion beams in order to achieve better torsion flexibili However there is a limitation of the torsion beam width. From shutter arrays fabricated with different torsion bea widths, the shutter arrays with 3μm wide torsion beams showed greater stiffness than those with 2μm, especia when metal electrodes were deposited on shutters. As usually concerned, thermal oxide may introduce thermal stre that fractures the silicon-nitride membranes. Comparing the two types of silicon oxide used as

(a)

(b)

Figure 5. SEM images of (a) the front side and backside of a 32x32 microshutter array with zoom-in images, and (b) backside of a 128x128 microshutter arrays with zoom-in images.

the etch-stops, the thermal oxide did not generate too much thermal stress over the LPCVD oxide. As a result, t thermal oxide provided a better quality than the LPCVD oxide to protect shutter membrane from DRIE etching. T low-stress silicon nitride wafers from one source was proved having a better uniformity over those from other t sources. We have fabricated 32x32 shutter arrays and 128x128 shutter arrays and we are very close to fabric 512x512 arrays. A 32x32 and a 128x128 mechanical microshutter arrays are shown in figure 5(a) and 5(respectively.

2.2 Mechanical & Electrostatic actuated Shutter Arrays

Mechanical and electrostatic actuated shutter arrays are designed with a double-shutter mechanism. Figure 6 sho the operating sequence of a schematic double-shutter array and a prototypic 3x3 double-shutter array. A thin film aluminum in the thickness of 50nm is deposited on shutters as electrodes. An upper array and a lower array a aligned and brought in close contact. A voltage is applied to engage upper and lower shutters. A mechanical moti driven by precision-controlled step motors directs the upper array moving against the lower array in a directi shown in figure 6. The motion makes engaged shutter pixels open.

The engagement of upper and lower shutter pixels is addressed by a CMOS circuitry. Figure 7 shows a blo diagram of a 32x32 element CMOS-based addressing circuit and an image of a circuit device fabricated at Godda Space Flight Center. A decoding circuitry controls both vertical bit/bit-not lines and horizontal row lines through t array. A shutter driver array decodes the column address in the column decoder. A column clock locks the select data state for each column into the corresponding latch in the column data register. The selected row address decoded in the row decoder circuitry. A row clock locks the states from the bit lines into memory cells on t selected row. The CMOS processing involves: wafer oxidation; defining p-wells and ion implant boron; driving boron and growing oxide for implant mask; defining p+ source, drains, guard bands, and ion implant boron; defini n+ source, drains, guard bands, and ion implant phosphorous; etching off doped oxide and growing gate oxide; i implant boron to adjust the threshold voltages; depositing polysilicon for gate electrodes; depositing a second lay of polysilicon for interconnects; and etching the contact holes, depositing aluminum metallization for interconne and bonding pads. All CMOS circuits are fabricated on shutter frames. After CMOS processing, 50nm-thick lo stress silicon nitride is deposited on the wafer as a passivation film. Meanwhile, the low-stress silicon nitride is us as the active membrane for shutters. A second aluminum metallization in the thickness of 50nm is deposited shutter regions as electrodes for shutter actuation. Followed, is mechanical shutter array processing described Section 2.1.

Figure 6. Motion of mechanical- & electrostatic-actuated shutter arrays – the double shutter mechanism. Schematic openi sequence (left), and prototypic opening sequence (right)

Figure 7. A block diagram of a COMS-based addressing circuit (right) and an image of a circuit device fabricated at Godd Space Flight Center (left)

We investigated the etch profile, the uniformity, and the notching control in DRIE etching for mechanical shut arrays to be integrated with CMOS circuitry. The uniformity and notching control are more important than the et profile for those mechanical and electrostatic actuated shutter arrays. Shutter frame walls for these arrays a designed 10µm-thick in order to leave enough spaces for CMOS circuitry fabrication. The notching, i.e. the silic over-etching near shutter membranes when the DRIE etching reaches the end, may lead to silicon removal arou CMOS regions and cut into CMOS circuitry. Notching is caused by the bombardment of etching agents that hit shutter membranes and are scattered side-ways. Reducing the energy of etching agents helps notching control. W odified DRIE etching parameters by increasing cap pressure and reducing platen power. During DRIE etching, t etch rate can vary at different wafer locations due to ion density distribution. Typically, the etching close to wa edges runs faster than that close to wafer centers. The ununiformity of ion density distribution causes etchi ununiformity problems, which becomes severer when wafers with large size arrays are etched. The etchi uniformity can be improved by reducing cap pressure, but it is contradictory to the notching control. Therefore run DRIE etching in two steps. Low pressure is used in the first step when etching runs through the first 9(thickness of the shutter wafer, while high pressure is used in the second step through the last 10% of the wafer.

2.3 Magnetic & Electrostatic actuated Shutter Arrays

Magnetic and electrostatic actuation of shutter arrays was designed utilizing a single-shutter mechanism. T configuration of the actuation is shown in Figure 8 schematically. A shutter array is fabricated with a magnetic p on each shutter, and an electrical electrode strip on each row. A second electrode on the shutter array is located the backside of the frame. The shutter array is flipped over facing a substrate. The substrate is transparent w electrical electrode strips aligned with columns of the shutter array and perpendicular to electrode strips on shut rows. Shutters are able to open up 90 degree into shutter windows when a magnetic field is applied to the shut array. The magnet moves in a direction as shown in the figure so that the shutters open row by row. Applying voltage between selected electrode rows on the shutter array and columns on the substrate addresses the holding shutter close, while a voltage between selected electrode rows and the frame electrode fulfills the holding for shut open.

Opening

Shutter membrane

Shutter electrode

Magnetic pad

N

S S Magnet

Frame electrode

Silicon frame

Substrate electrode

Quartz substrate

Figure 8. Configuration of magnetic and electrostatic actuation for the single-shutter array mechanism

Magnetic pads and electrical electrodes are fabricated on shutter wafers prior to mechanical shutter processi Metal thin-films are grown on shutter wafers through a sputtering deposition and form a tri-layer metallization. T tri-layer consists of 100nm-thick aluminum as the shutter electrical electrodes, 200nm-thick magnetic material as t magnetic pads, and 5nm-thick aluminum as a passivation film to protect magnetic pads. Magnetic pads a lithographically patterned on all shutters. Microshutters themselves are then patterned starting with an alumin etch, which defines shutter electrode rows and also microshutter blades and frames. Followed is a RIE etchi through the silicon nitride, which is the first step of mechanical microshutter processing described in section 2 The electrodes on the backside of shutter wafers are processed by an E-beam deposition of 5nm-thick Ti a 200nm-thick Au after wafer thinning and before backside shutter window patterning. In the development sta quartz wafers are selected as the substrate material for its fair transparency to infrared. In the future, materials w higher transparency to infrared, such as CaF_2, will be used for final production,. For the same reason a thin film chromium silicide is deposited on substrates and patterned for substrate electrodes. The substrate is then passivat by depositing a thin layer of silicon nitride to prevent shorting between electrodes on shutter arrays and substrates. Through a lift-off process, pads on the substrate are the only areas kept from the silicon nitri passivation. Some pads are then bonded to the pads on shutter arrays and others are used as wire bonding pads packaging.

Thermal stress introduced by the mismatch of thermal expansion coefficient between a metal and a silicon-nitri thin films may cause shutters bowing. Co, Co(50)Fe(50), and Co(90)Fe(10) were tested as the material candida for magnetic pads. They were deposited on shutter arrays by plasma sputtering. Co(90)Fe(10) films showed the le bowing and therefore the least thermal stresses. Magnetic actuation was tested by applying a magnetic field shutter arrays. Figure 9 shows optical images of shutters in (a) an closing position and (b) an opening position. T dark areas shown in Figure 9(b) were shutters opening at different angles. The image indicated that the magnet shutter actuation was moved to the position underneath shutters in the third column from right where shutt opened 90 degrees out of plane. The effect of magnetic pad sizes on thermal stresses and magnetic saturation under investigation.

(a)

(b)

One of the advantages of the single-shutter mechanism over the double-shutter mechanism is further increasing t fill factor. The width of shutter frames can be reduced from 10μm to 1~2μm because CMOS circuitry may not needed. The etch profile (side wall profile) control in the DRIE etching process then becomes a more importa aspect for magnetic and electrostatic actuated shutter arrays. We are working on the modification of DRIE etchi recipes to minimize the width of shutter frames.

3. Summary and Future Work

Microshutter arrays were designed as an object selector for Multi-Object Spectrometer on the Next Generati Space Telescope. Microshutter arrays are transmissive devices minimizing light scattering and so allowing hi contrast of spectroscopy. We have fabricated 32x32 and 128x128 mechanical microshutter arrays with 100x100μ pixels using combined conventional semiconductor processing and MEMS technologies. We have developed t microshutter actuation/addressing mechanisms: mechanical and electrostatic actuation – the double shut mechanism, and magnetic and electrostatic actuation – the single shutter mechanism. For the fabrication microshutter arrays with mechanical and electrostatic actuation, we integrated CMOS circuitry for addressi mechanical carrier stage for actuation, and electrical holding electrodes into microshutter processing. Shutter arra with 10μm-wide or less frames were fabricated with improved uniformity and notching control during DR etching. For the fabrication of microshutter arrays with magnetic and electrostatic actuation, we have integrat magnetic circuitry for actuation, and electrical circuitry for addressing and holding, into microshutter ar processing. Materials for shutter membranes, oxide etch-stop, magnetic pads, electrodes and bonding pads ha been tested and selected. We are working on the fabrication of microshutter arrays with 2μm-wide frames improve the fill factor of shutter array devices.

We are close to fabricating 512x512 microshutter arrays with full actuation and addressing functions. We plan develop 2048x2048 microshutter arrays as a mosaic of 16 512x512 arrays with a supporting frame between t arrays. Functional testing will be carried out in a controllable cryogenic environment in the near future.

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October 2001 · Proceedings of SPIE - The International Society for Optical Engineering

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January 2003

Magnetically actuated MEMS microshutter arrays are being developed at the NASA Goddard Space Flight Center for use in a multi-object spectrometer on the James Webb Space Telescope (JWST), formerly Next Generation Space Telescope (NGST). The microshutter arrays are designed for the selective transmission of light with high efficiency and high contrast. The JWST environment requires cryogenic... [Show full abstract]

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