LMR10530 SIMPLE SWITCHER® 5.5Vin, 3.0A Step-Down Voltage Regulator in WSON-10

Check for Samples: LMR10530

FEATURES

- **Input Voltage Range of 3.0V to 5.5V**
- **Output Voltage Range of 0.6V to 4.5V**
- **1.5 MHz (LMR10530X) and 3 MHz (LMR10530Y) Switching Frequencies**
- **WSON-10 (3 x 3 x 0.8 mm) Packaging**
- **3.0A Steady-State Output Current**
- **Low Shutdown Iq, 300 nA Typical**
- **56mΩ PMOS Switch**
- **Internal Soft-Start**
- **Internally Compensated Peak Current-Mode Control**
- **Cycle-by-cycle Current Limit and Thermal Shutdown**
- **WEBENCH® enabled**

PERFORMANCE BENEFITS

- **Extremely Easy to Use**
- **Tiny Overall Solution Reduces System Cost**

APPLICATIONS

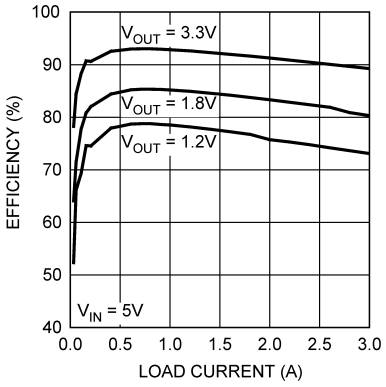
- **Point-of-load Conversions from 3.3V and 5V Rails**
- **Space Constrained Applications**

DESCRIPTION

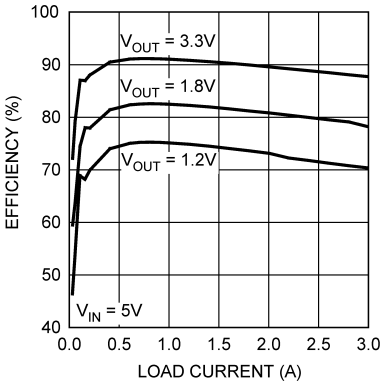
The LMR10530 regulator is a monolithic, high frequency, PWM step-down DC/DC converter available in a 10-pin WSON package. It contains all the active functions to provide local DC/DC conversion with fast transient response and accurate regulation in the smallest possible PCB area. With a minimum of external components, the LMR10530 is easy to use. The ability to drive 3.0A loads with an internal 56 mΩ PMOS switch using state-of-the-art 0.5µm BiCMOS technology results in the best power density available. The control circuitry allows on-times as low as 30ns, thus supporting exceptionally high frequency conversion over the entire 3V to 5.5V input operating range down to the minimum output voltage of 0.6V. Switching frequency is internally set to 1.5MHz or 3.0MHz, allowing the use of extremely small surface mount inductors and capacitors. Even though the operating frequency is high, efficiencies up to 93% are easy to achieve. External shutdown is included, featuring an ultra-low stand-by current of 300nA. The LMR10530 utilizes peak current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce inrush current, cycle-by-cycle current limit, frequency foldback, thermal shutdown, and output over-voltage protection.

System Performance

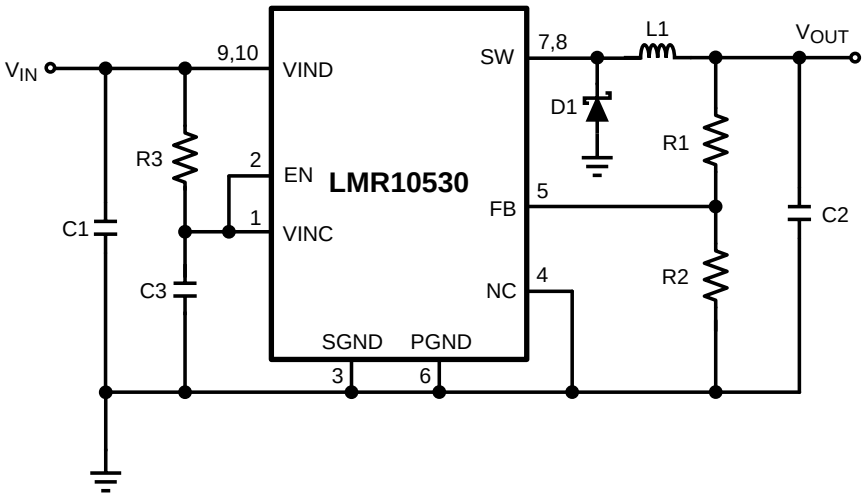
Efficiency vs Load Current
LMR10530X V_{IN} = 5V



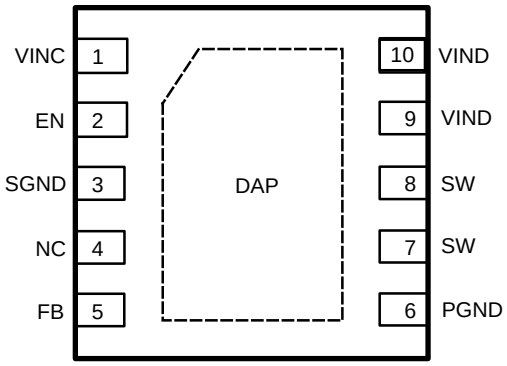
Efficiency vs Load Current
LMR10530Y V_{IN} = 5V



Typical Application Circuit



Connection Diagram



10-Pin WSON
See Package Number DSC

PIN DESCRIPTIONS

Pin(s)	Name	Description
1	VINC	Input supply for internal bias and control circuitry. Need to locally bypass this pin to GND.
2	EN	Enable control input. Logic high enables operation. Do not allow this pin to float or subject to voltages greater than V_{IN} + 0.3V.
3	SGND	Signal (analog) ground. Place the bottom resistor of the feedback network as close as possible to this pin for good load regulation.
4	NC	No user function, connect this pin to GND.
5	FB	Feedback pin. Connect this pin to the external resistor divider to set output voltage.
6	PGND	Power ground pin. Provides ground return path for the internal driver.
7, 8	SW	Switch pins. Connect these pins to the inductor and catch diode.
9, 10	VIND	Input supply voltage. Connect a bypass capacitor locally from these pins to PGND.
DAP	Die Attach Pad	Connect to system ground for low thermal impedance, but it cannot be used as a primary GND connection.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

VINC, VIND	-0.5V to 7V
FB Voltage	-0.5V to 3V
EN Voltage	-0.5V to V_{IN}+o.3V
SW Voltage	-0.5V to 7V
ESD Susceptibility(3)	2kV
Junction Temperature(4)	150°C
Storage Temperature	-65°C to +150°C
Soldering Information Infrared/Convection Reflow (15sec)	220°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.
(4) Thermal shutdown will occur if the junction temperature exceeds the maximum junction temperature of the device.

Operating Ratings

VINC, VIND	3V to 5.5V
Junction Temperature	-40°C to +125°C

Electrical Characteristics

Unless otherwise specified under the **Conditions** column, V_{IN} = 5V. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage	WSON-10 Package	**0.588**	0.600	**0.612**	V
$\Delta V_{FB}/(\Delta V_{IN} x V_{FB})$	Feedback Voltage Line Regulation	V_{IN} = 3V to 5.5V		0.08		%/V
I_B	Feedback Input Bias Current			0.1	**100**	nA
UVLO	Undervoltage Lockout	V_{IN} Rising		2.70	**2.90**	V
		V_{IN} Falling	**1.85**	2.35		
	UVLO Hysteresis			0.35		V
f_{SW}	Switching Frequency	LMR10530X	**1.1**	1.5	**1.95**	MHz
		LMR10530Y	**2.25**	3.0	**3.75**	
D_{MAX}	Maximum Duty Cycle	LMR10530X	**86**	95		%
		LMR10530Y	**80**	90		
D_{MIN}	Minimum Duty Cycle	LMR10530X		5		%
		LMR10530Y		7		
$R_{DS(ON)}$	Switch On Resistance			58	**90**	mΩ
I_{CL}	Switch Current Limit		**3.4**	4.4		A
V_{EN_TH}	Enable Threshold Voltage		**1.8**			V
	Shutdown Threshold Voltage				**0.4**	
I_{SW}	Switch Leakage			100		nA
I_{EN}	Enable Pin Current	Sink/Source		100		nA
I_Q	Quiescent Current (switching)	LMR10530X, V_{FB} = 0.55		3.2	**5**	mA
		LMR10530Y, V_{FB} = 0.55		4.3	**6.5**	
	Quiescent Current (shutdown)	All Options V_{EN} = 0V		300		nA
V_{FB_F}	FB Frequency Foldback Threshold	All Options		0.32		V
f_{FB}	Foldback Frequency	LMR10530X, V_{FB} = 0V		400		kHz
		LMR10530Y, V_{FB} = 0V		800		
θ_{JA}	Junction to Ambient 0 LFPM Air Flow (1)			53		°C/W
θ_{JC}	Junction to Case (1)			12		°C/W
T_{SD}	Thermal Shutdown Threshold (2)	Junction Temperature Rising		165		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis	Junction Temperature Falling		15		°C

(1) Applies for packages soldered directly onto a 4” x 3” 4-layer standard JEDEC board in still air.
(2) Thermal shutdown will occur if the junction temperature exceeds the maximum junction temperature of the device.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, V_{IN} = 5V and T_A = 25°C

Efficiency vs Load Current - "LMR10530X" and "LMR10530Y"

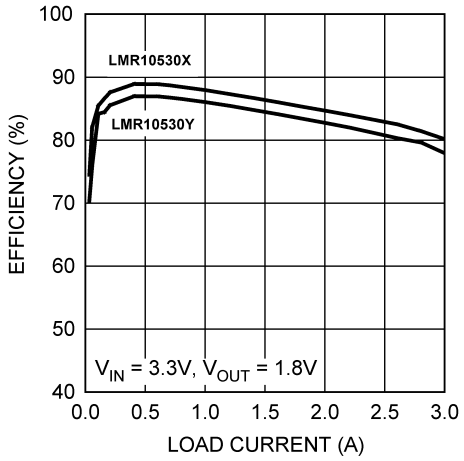


Figure 1.

Efficiency vs Load Current - "LMR10530X"

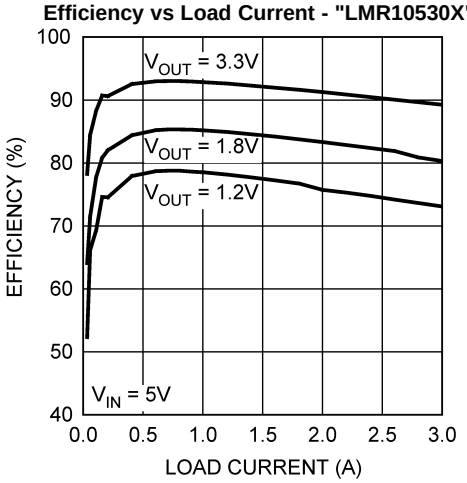


Figure 2.

Efficiency vs Load Current - "LMR10530Y"

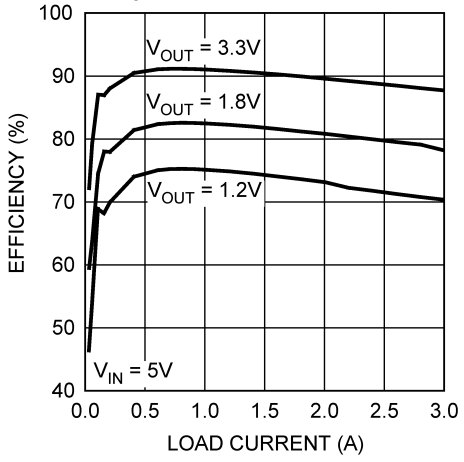


Figure 3.

Oscillator Frequency vs Temperature - "LMR10530X"

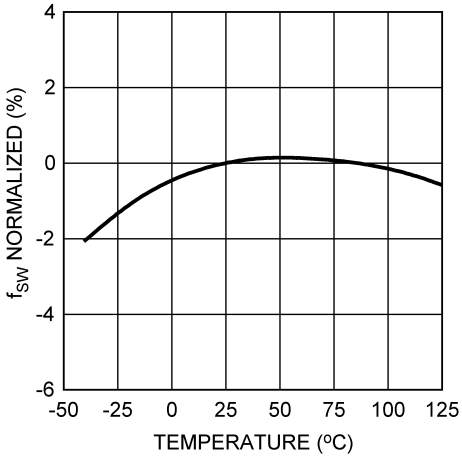


Figure 4.

Oscillator Frequency vs Temperature - "LMR10530Y"

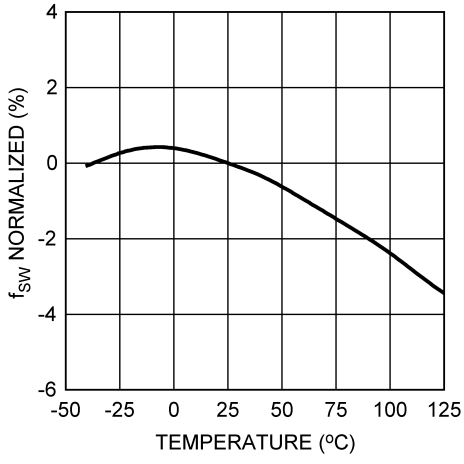


Figure 5.

Current Limit vs Temperature

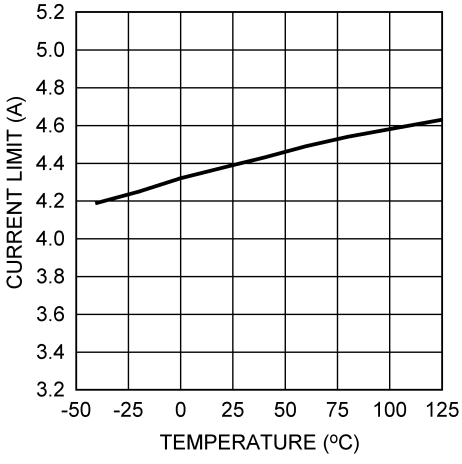


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} = 5V and T_A = 25°C

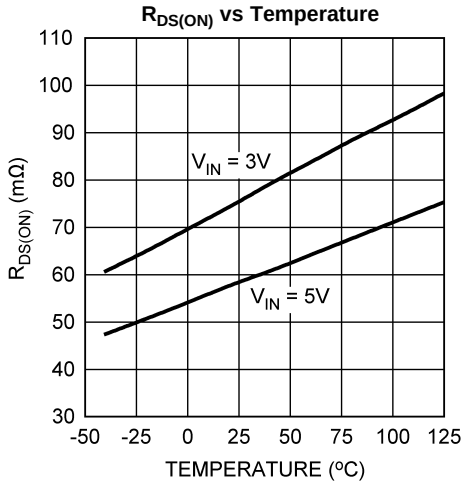


Figure 7.

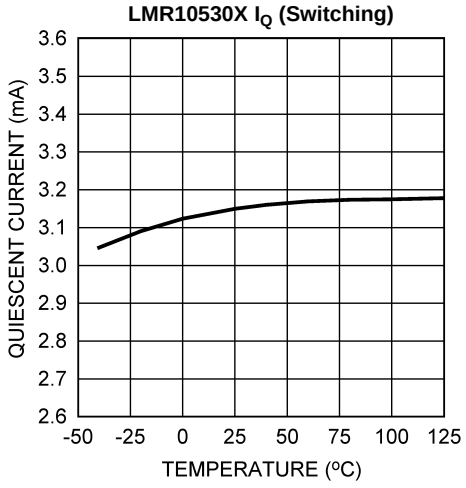


Figure 8.

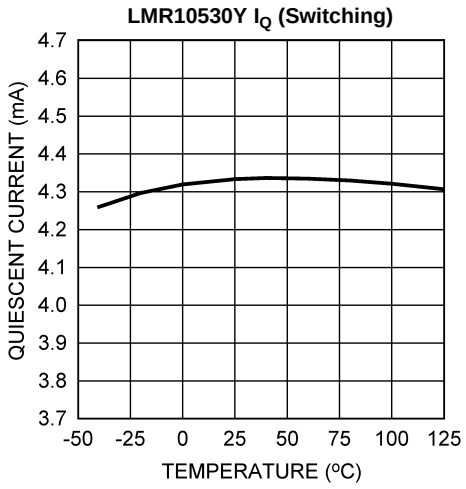


Figure 9.

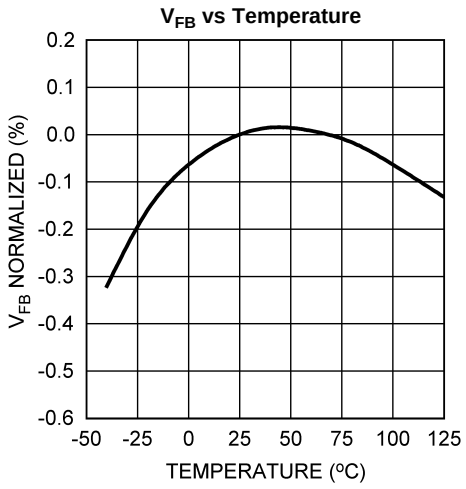


Figure 10.

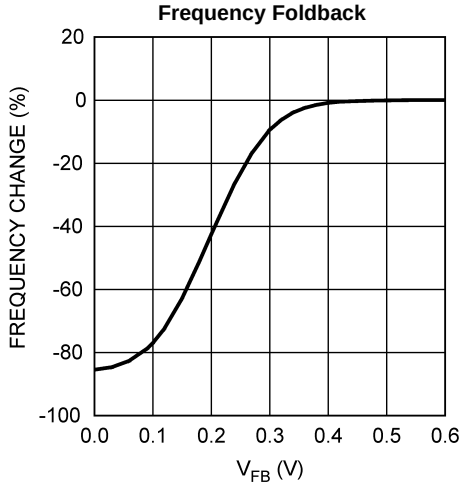


Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} = 5V and T_A = 25°C.

Loop Gain and Phase - "LMR10530X"

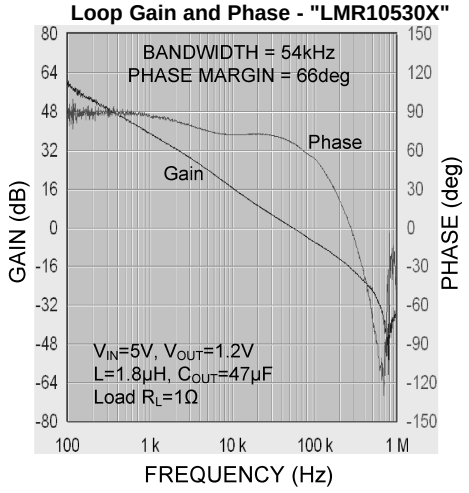


Figure 12.

Loop Gain and Phase - "LMR10530Y"

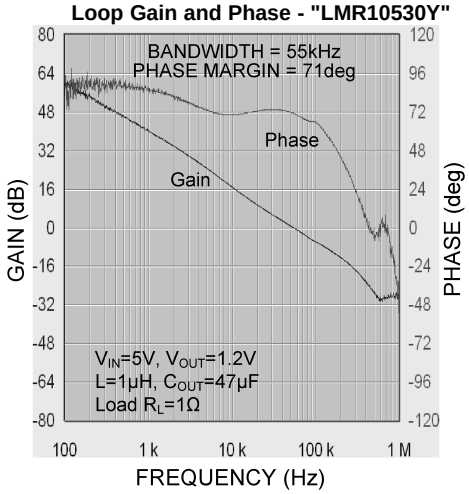


Figure 13.

Load Step Response - "LMR10530X"

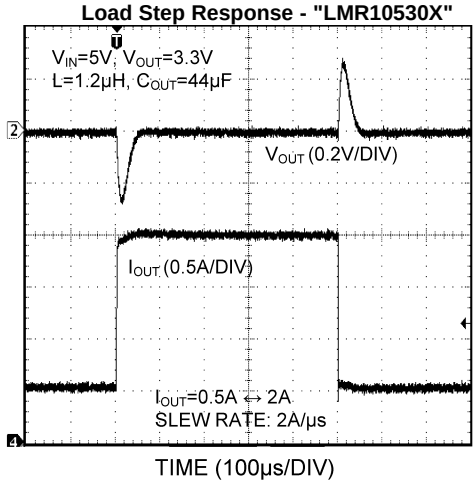


Figure 14.

Line Transient Response - "LMR10530X"

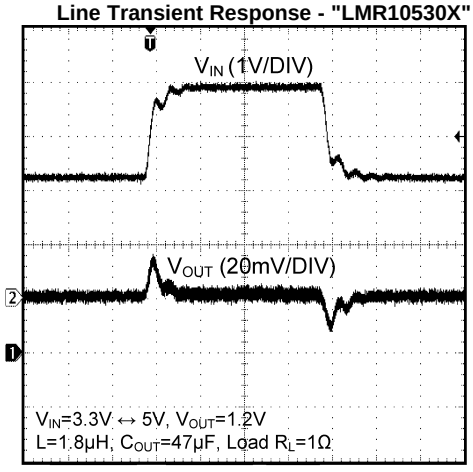


Figure 15.

Startup by EN - "LMR10530X"

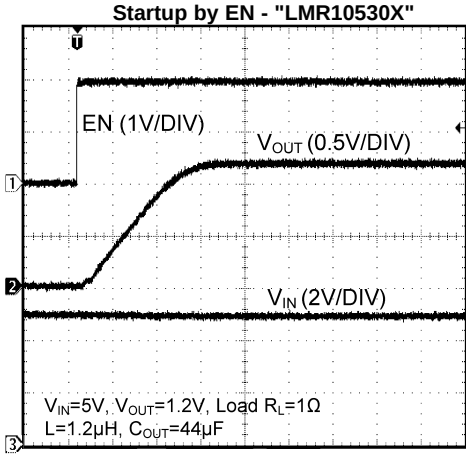


Figure 16.

Shutdown by EN - "LMR10530X"

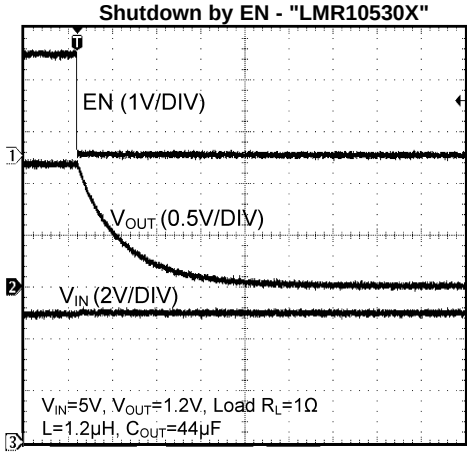
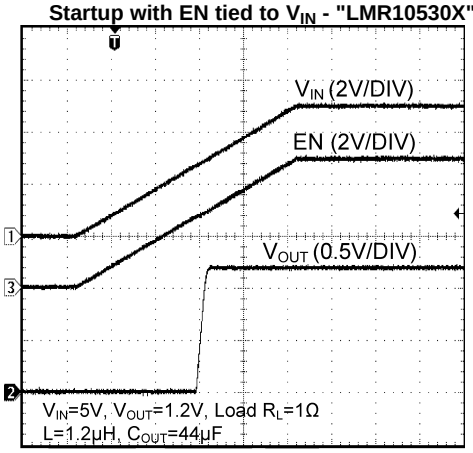


Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} = 5V and T_A = 25°C

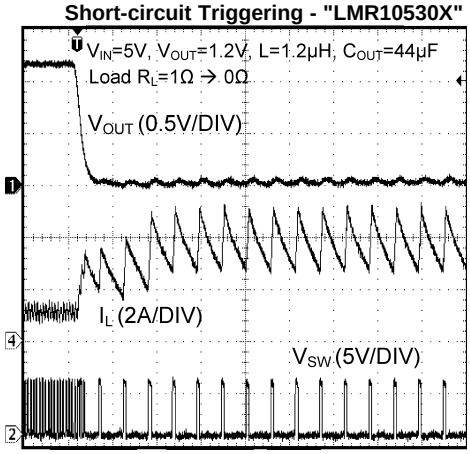
Startup with EN tied to V_{IN} - "LMR10530X"



TIME (2ms/DIV)

Figure 18.

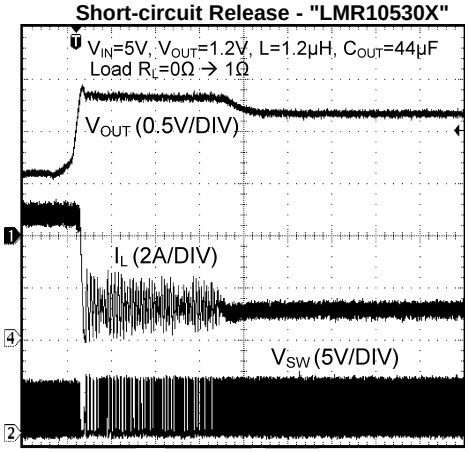
Short-circuit Triggering - "LMR10530X"



TIME (10µs/DIV)

Figure 19.

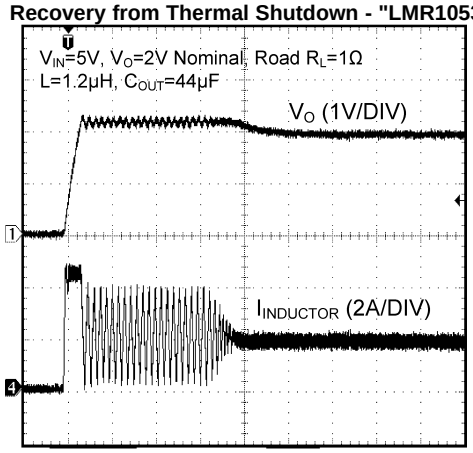
Short-circuit Release - "LMR10530X"



TIME (40µs/DIV)

Figure 20.

Recovery from Thermal Shutdown - "LMR10530X"



TIME (40µs/DIV)

Figure 21.

Block Diagram

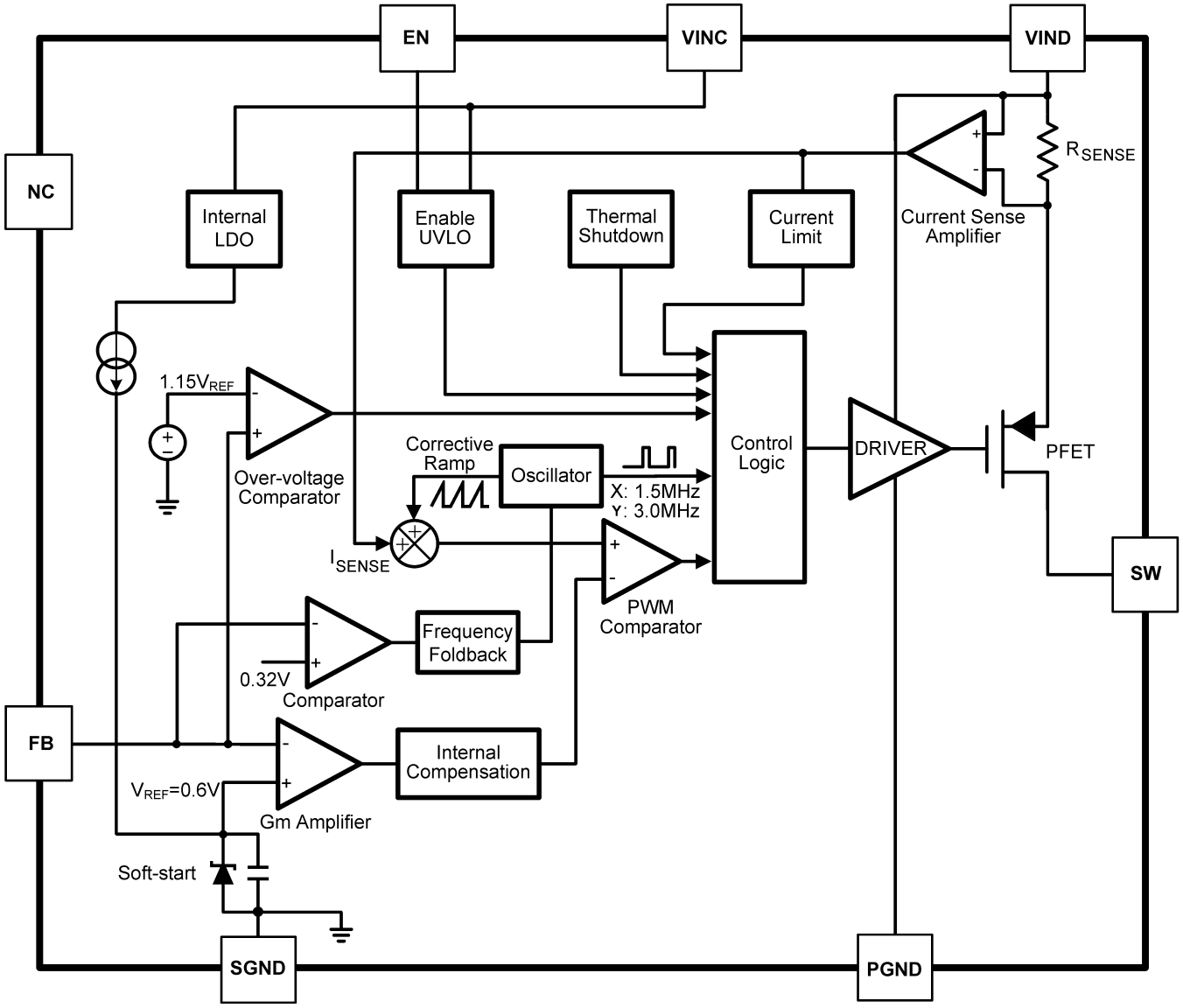


Figure 22. Simplified Block Diagram

APPLICATION INFORMATION

THEORY OF OPERATION

The LMR10530 is a constant frequency PWM buck regulator IC that delivers a 3.0A load current. The regulator is available in preset switching frequencies of 1.5MHz or 3.0MHz. This high frequency allows the LMR10530 to operate with small surface mount capacitors and inductors, resulting in a DC/DC converter that requires a minimum amount of board space. The LMR10530 is internally compensated, therefore it is simple to use and requires few external components. The LMR10530 uses peak current-mode control to regulate the output voltage. The following description of operation of the LMR10530 will refer to the Typical Application Circuit, to the waveforms in Figure 23 and simplified block diagram in Figure 22. The LMR10530 supplies a regulated output voltage by switching the internal PMOS power switch at a constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal PMOS power switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the internal power switch turns off until the next switching cycle begins. During the switch off-time, the inductor current discharges through the catch diode D1, which forces the SW pin to swing below ground by the forward voltage (V_D) of the catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

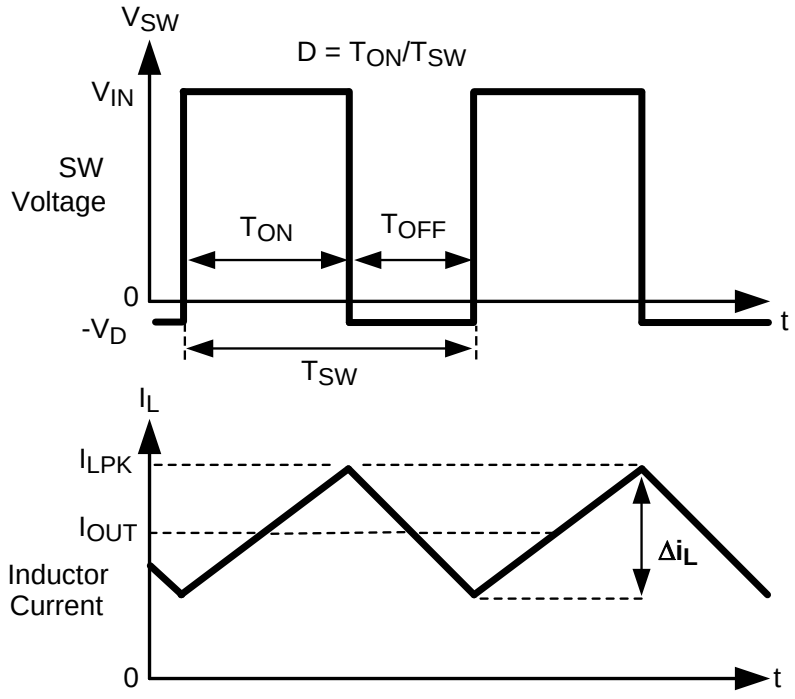


Figure 23. SW Pin Voltage and Inductor Current Waveforms

SOFT-START/SHUTDOWN

The LMR10530 has both enable and shutdown modes that are controlled by the EN pin. Connecting a voltage source greater than 1.8V to the EN pin enables the operation of the LMR10530, while reducing this voltage below 0.4V places the part in a low quiescent current (300nA typical) shutdown mode. There is no internal pull-up on EN pin, therefore an external signal is required to initiate switching. Do not allow this pin to float or rise to 0.3V above V_{IN}. It should be noted that when the EN pin voltage rises above 1.8V while the input voltage is greater than UVLO, there is 15µs delay before switching starts. During this delay the LMR10530 will go through a power on reset state after which the internal soft-start process commences. During soft-start, the error amplifier's reference voltage ramps from 0V to its nominal value of 0.6V in approximately 600µs. This forces the regulator output to ramp up in a controlled fashion, which helps reduce inrush current seen at the input and minimizes output voltage overshoot.

The simplest way to enable the operation of the LMR10530 is to connect the EN pin to V_{IN} which allows self start-up of the LMR10530 whenever the input voltage is applied. However, when an input voltage of slow rise time is used to power the application and if both the input voltage and the output voltage are not fully established before the soft-start time elapses, the control circuit will command maximum duty cycle operation of the internal power switch to bring up the output voltage rapidly. When the feedback pin voltage exceeds 0.6V, the duty cycle will have to reduce from the maximum value accordingly, to maintain regulation. The reduction of duty cycle takes a finite amount of time and can result in a transient in output voltage for a short duration, as shown in Figure 24. In applications where this output voltage overshoot is undesirable, one simple solution is to add a feed-forward capacitor C_{FF}) across the top feedback resistor R1 to speed Gm Amplifier recovery. In practice, a 27nF to 100nF ceramic capacitor is usually a good choice to remove the overshoot completely or limit the overshoot to an insignificant level during startup, as shown in Figure 25. Another more effective solution is to control EN pin voltage by a separate logic signal, and pull the signal high only after V_{IN} is fully established. In this way, the chip can execute a normal, complete soft start process, minimizing any output voltage overshoot. Under some circumstances at cold temperature, this approach may also be required to minimize any unwanted output voltage transients that may occur when the input voltage rises slowly. For a fast rising input voltage (100µs for example), there is no need to control EN separately or add a feed-forward capacitor since the soft-start can bring up output voltage smoothly as shown in Figure 26.

During startup, the LMR10530 gradually increases the switching frequency from 400kHz (LMR10530X) or 800kHz (LMR10530Y) to the nominal fixed value, as the feedback voltage increases (see Frequency Foldback section for more information). Since the internal corrective ramp signal adjusts its slope dynamically, and is proportional to the switching frequency during startup, a larger output capacitance may be required to insure a smooth output voltage rise, at low programmed output voltage and high output load current.

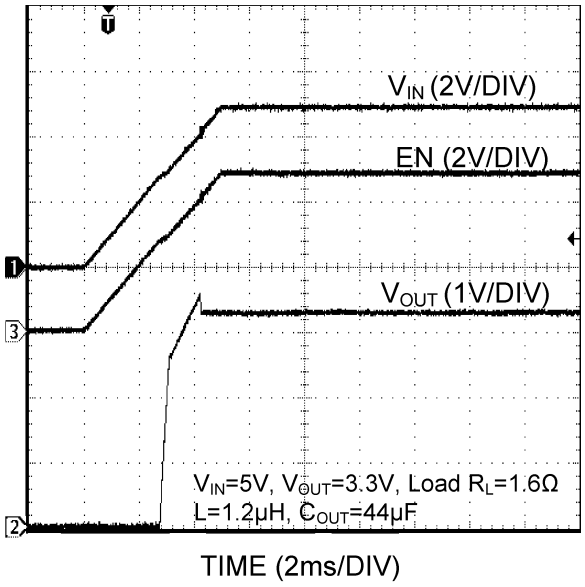


Figure 24. Startup Response to V_{IN}

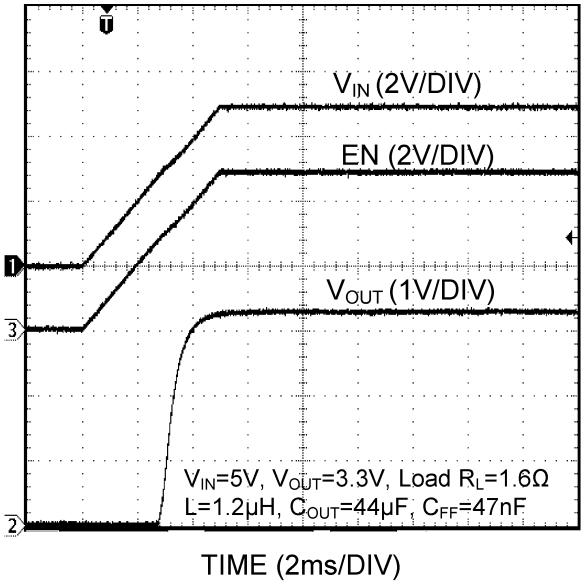


Figure 25. Startup Response to V_{IN} with C_{FF}

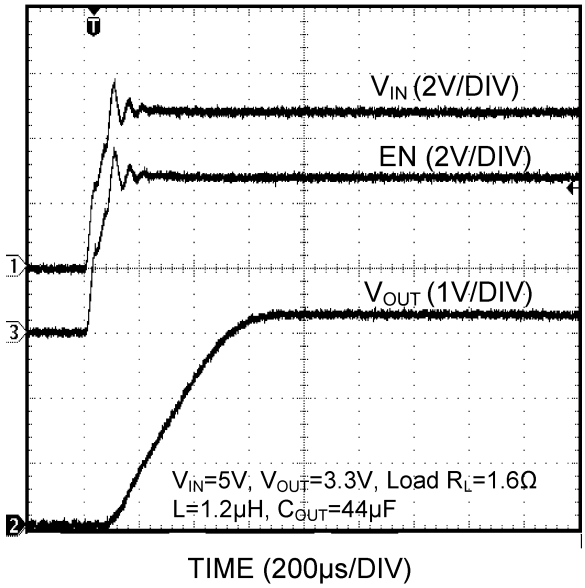


Figure 26. Startup Response to V_{IN} with 100µs rise time

FREQUENCY FOLDBACK

The LMR10530 uses frequency foldback to help limit switch current and power dissipation during start-up, short-circuit and over load conditions by sensing if the feedback voltage is below 0.32V (typical). The LMR10530 will reduce the switching frequency from the nominal fixed value (1.5MHz or 3.0MHz) down to 400kHz (LMR10530X) or 800kHz (LMR10530Y) when the feedback voltage drops to 0V. See the Frequency Foldback plot in the Typical Performance Characteristics section.

LOAD STEP RESPONSE

The LMR10530 has a fixed internal loop compensation, which results in a small-signal loop bandwidth highly related to the output voltage level. In general, the loop bandwidth at low voltage is larger than at high voltage due to the increased overall loop gain. The limited bandwidth at high output voltage may pose a challenge when loop step response is concerned. In this case, one effective approach to improving loop step response is to add a feed-forward capacitor (C_{FF}) in the range of 27nF to 100nF in parallel with the upper feedback resistor (assuming the lower feedback resistor is 2kΩ), as shown in Figure 27. The feed-forward capacitor introduces a zero-pole pair which helps compensate the loop. The position of the zero-pole pair is a function of the feedback resistors and capacitor:

$$\omega_z = \frac{1}{R1 \times C_{FF}} \text{ (rad/s)} \quad (1)$$

$$\omega_p = \frac{1}{R1 \times C_{FF}} \left(1+\frac{R1}{R2}\right) \text{ (rad/s)} \quad (2)$$

Note the factor in parenthesis is the ratio of the output voltage to the feedback voltage. As the output voltage gets close to 0.6V, the pole moves towards the zero, tending to cancel it out. Consequently, adding C_{FF} will have less effect on the step response at lower output voltages.

As an example, Figure 29 shows that at the output voltage of 3.3V, a 47nF of C_{FF} can boost the loop bandwidth to 117kHz, from the original 23kHz as shown in Figure 28. Correspondingly, the responses to a load step between 0.3A and 3A without and with C_{FF} are shown in Figure 30 and Figure 31 respectively. The higher loop bandwidth as a result of C_{FF} reduces the total output excursion by more than half.

Aside from the above approach, increasing the output capacitance is generally also effective to reduce the excursion in output voltage caused by a load step. This approach remains valid for applications where the desired output voltages are close to the feedback voltage.

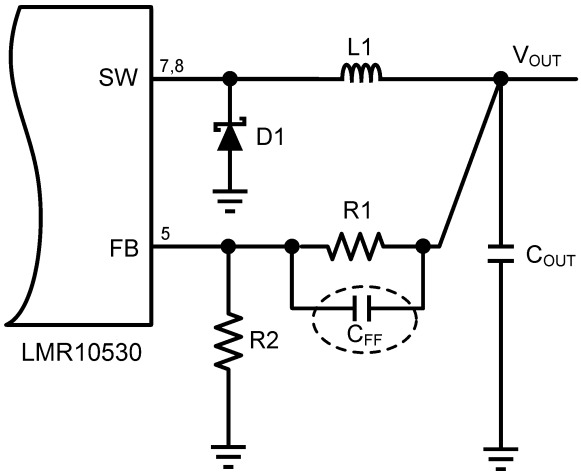


Figure 27. Adding a C_{FF} Capacitor

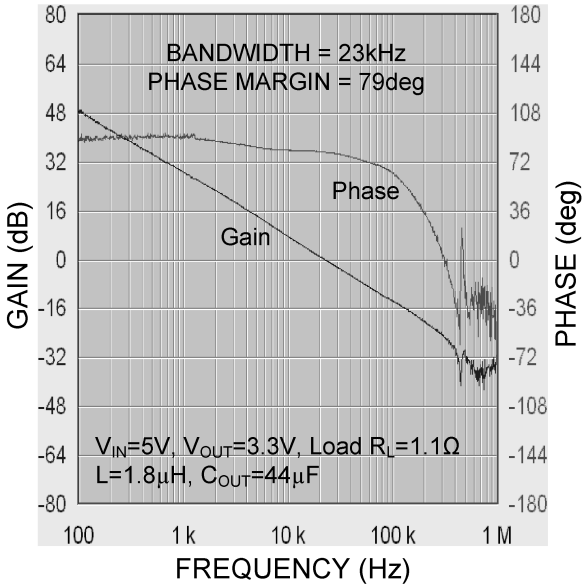


Figure 28. Loop Gain and Phase without C_{FF}

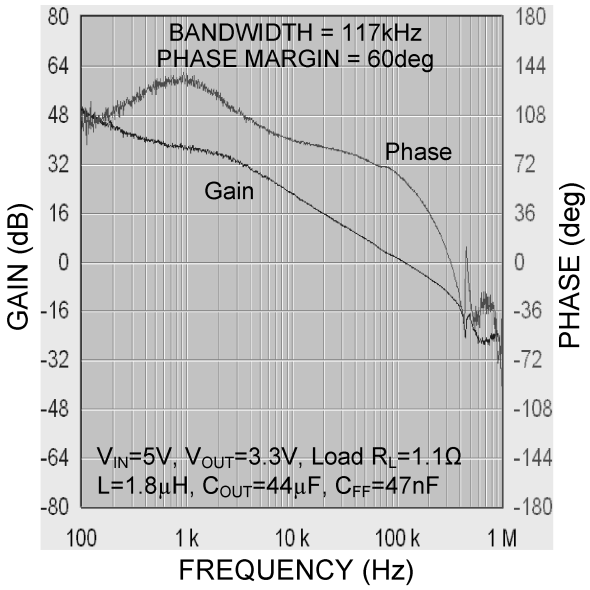


Figure 29. Loop Gain and Phase with C_{FF}

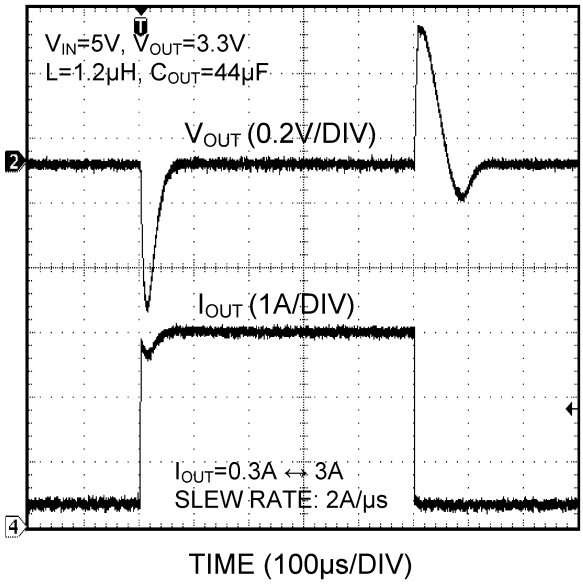


Figure 30. Load Step Response without C_{FF}

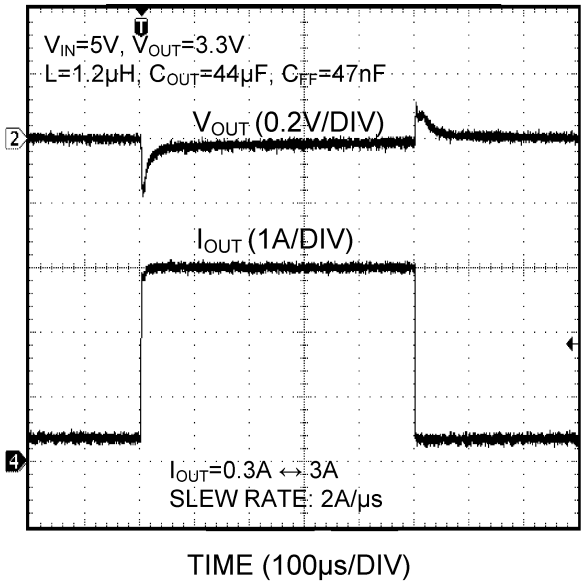


Figure 31. Load Step Response with C_{FF}

OUTPUT OVER-VOLTAGE PROTECTION

The LMR10530 has a built in output over-voltage comparator that compares the FB pin voltage to a threshold voltage that is 15% higher than the internal reference V_{REF}. Once the FB pin voltage exceeds this threshold level (typically 0.69V), the internal PMOS power switch is turned off, which allows the output voltage to decrease towards regulation.

UNDER-VOLTAGE LOCKOUT

Under-voltage lockout (UVLO) prevents the LMR10530 from operating until the input voltage exceeds 2.70V (typical). The UVLO threshold has approximately 350mV of hysteresis, so the part will operate until V_{IN} drops below 2.35V (typical). Hysteresis prevents the part from turning off during power up if V_{IN} is non-monotonic.

CURRENT LIMIT

The LMR10530 uses cycle-by-cycle current limiting to protect the internal power switch. During each switching cycle, a current limit comparator detects if the power switch current exceeds 4.4A (typical), and turns off the switch until the next switching cycle begins.

THERMAL SHUTDOWN

Thermal shutdown limits total power dissipation by turning off the internal power switch when the IC junction temperature typically exceeds 165°C. After thermal shutdown occurs, the power switch does not turn on again until the junction temperature drops below approximately 150°C.

Design Guide

INDUCTOR SELECTION

The Duty Cycle (D) can be approximated quickly using the ratio of output voltage (V_{OUT}) to input voltage (V_{IN}):

$$D = \frac{V_{OUT}}{V_{IN}} \tag{3}$$

The catch diode (D1) forward voltage drop and the voltage drop across the internal PMOS must be included to calculate a more accurate duty cycle. Calculate D by using the following formula:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \tag{4}$$

V_{SW} can be approximated by:

$$V_{SW} = I_{OUT} \times R_{DS(ON)} \tag{5}$$

where

- I_{OUT} is output load current.

The diode forward drop (V_D) can range from 0.3V to 0.7V depending on the quality of the diode. The lower the V_D, the higher the operating efficiency of the converter.

The inductor value determines the output ripple current (Δi_L, as defined in Figure 23). Lower inductor values decrease the size of the inductor, but increase the output ripple current. An increase in the inductor value will decrease the output ripple current. In general, the ratio of ripple current to the output current is optimized when it is set between 0.2 and 0.4 for output currents above 2A. This ratio r is defined as:

$$r = \frac{\Delta i_L}{I_{OUT}} \tag{6}$$

One must ensure that the minimum current limit (3.4A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by:

$$I_{LPK} = I_{OUT} + \Delta i_L/2 \tag{7}$$

When the designed maximum output current is reduced, the ratio r can be increased. At a current of 0.1A, r can be made as high as 0.9. The ripple ratio can be increased at lighter loads because the net ripple is actually quite low, and if r remains constant the inductor value can be made quite large. An equation empirically developed for the maximum ripple ratio at any current below 2A is:

$$r = 0.387 \times I_{OUT}^{-0.3667} \tag{8}$$

Note that this is just a guideline, and it needs to be combined with two important factors for proper selection of inductance values at any operating condition. The first consideration is at output voltage above 2.5V, one needs to ensure that the inductance given by the above guideline should not be less than 1µH for the LMR10530X or 0.5µH for the LMR10530Y. Since the LMR10530 has a fixed internal corrective ramp signal, a very low inductance value at high output voltage will generate a very steep down slope of inductor current, which will result in an insufficient slope compensation, and cause instability known as sub-harmonic oscillation. Another consideration is at low load current, one needs to ensure that the inductance value given by the guideline should not exceed 10µH for the LMR10530X and 4.7µH for the LMR10530Y, since too much inductance effectively flattens the down slope of the inductor current, and may significantly limit the system bandwidth and phase margin resulting in instability.

The LMR10530 operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. See the Output Capacitor section for more details on calculating output voltage ripple.

Now that the ripple current is determined, the inductance is calculated by:

$$L = \frac{V_{OUT} + V_D}{I_{OUT} \times r \times f_{SW}} \times (1\text{-}D) \quad (9)$$

where

- f_{SW} is the switching frequency.

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating properly. Because of the operating frequency of the LMR10530, ferrite based inductors are preferred to minimize core losses. This presents little restriction since the variety and availability of ferrite-based inductors is large. Lastly, inductors with lower series resistance (DCR) will provide better operating efficiency. For recommended inductor selection, refer to Design Examples.

INPUT CAPACITOR

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage rating, RMS current rating, and ESL (Equivalent Series Inductance). The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating ($I_{RMS\text{-}IN}$) must be greater than:

$$I_{RMS\text{-}IN} = I_{OUT} \times \sqrt{D \times \left(1 - D + \frac{r^2}{12}\right)} \quad (10)$$

Neglecting inductor ripple simplifies the above equation to:

$$I_{RMS\text{-}IN} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad (11)$$

It can be shown from the above equation that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle D is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. As a rule of thumb, a large leaded capacitor will have high ESL and a 1206 ceramic chip capacitor will have very low ESL. At the operating frequencies of the LMR10530, leaded capacitors may have an ESL so large that the resulting impedance ($2\pi fL$) will be higher than that required to provide stable operation. It is strongly recommended to use ceramic capacitors due to their low ESR and low ESL. A 22µF multilayer ceramic capacitor (MLCC) is a good choice for most applications. In cases where large capacitance is required, use surface mount capacitors such as Tantalum capacitors and place at least a 4.7µF ceramic capacitor close to the V_{IN} pin. For MLCCs it is recommended to use X7R or X5R dielectrics. Consult capacitor manufacturer datasheet to see how rated capacitance varies over operating conditions.

OUTPUT CAPACITOR

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is:

$$\Delta V_{OUT} = \Delta I_L \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (12)$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LMR10530, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic capacitances in the inductor to the output. A ceramic capacitor will bypass this noise while a tantalum will not. Since the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications will require a minimum of 22µF output capacitance. In the case of low output voltage, a

larger output capacitance is required to ensure sufficient phase margin. Capacitance can often, but not always, be increased significantly with little detriment to the regulator stability. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R types. Again, verify actual capacitance at the desired operating voltage and temperature. Check the RMS current rating of the capacitor. The maximum RMS current rating of the capacitor is:

$$I_{RMS\text{-}OUT} = I_{OUT} \times \frac{r}{\sqrt{12}} \quad (13)$$

One may select a 1206 size MLCC for output capacitor, since its current rating is typically above 1A, more than enough for the requirement.

CATCH DIODE

The catch diode conducts during the switch off-time. A Schottky diode is recommended for its fast switching time and low forward voltage drop. The catch diode should be chosen such that its current rating is greater than:

$$I_D = I_{OUT} \times (1\text{-}D) \quad (14)$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency, choose a Schottky diode with a low forward voltage drop.

OUTPUT VOLTAGE

The output voltage is set using the following equation where R2 is connected between the FB pin and GND, and R1 is connected between V_{OUT} and the FB pin. A good value for R2 is 2kΩ.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (15)$$

$$V_{REF} = 0.60V \quad (16)$$

EFFICIENCY ESTIMATION

The complete LMR10530 DC/DC converter efficiency can be calculated in the following manner:

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (17)$$

Or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (18)$$

Calculations for determining the most significant power losses are shown below. Other losses totaling less than 2% are not discussed.

The main power loss (P_{LOSS}) in the converter includes two basic types of losses: switching loss and conduction loss. In addition, there is loss associated with the power required for the internal circuitry of IC. Conduction losses usually dominate at higher output loads, whereas switching losses dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D):

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \quad (19)$$

V_{SW} is the voltage drop across the internal power switch when it is on, and is equal to:

$$V_{SW} = I_{OUT} \times R_{DS(ON)} \quad (20)$$

V_D is the forward voltage drop across the catch diode. It can be obtained from the diode manufactures Electrical Characteristics section. If the DC voltage drop across the inductor (V_{DCR}) is accounted for, the equation becomes:

$$D = \frac{V_{OUT} + V_D + V_{DCR}}{V_{IN} + V_D - V_{SW}} \quad (21)$$

The conduction losses in the catch diode are calculated as follows:

$$P_{DIODE} = V_D \times I_{OUT} \times (1\text{-}D) \quad (22)$$

Often this is the single most significant power loss in the circuit. Care should be taken to choose a Schottky diode with a low forward voltage drop.

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to:

$$P_{IND} = I_{OUT}^2 \times R_{DCR} \quad (23)$$

The LMR10530 conduction loss is mainly associated with the internal power switch:

$$P_{COND} = (I_{OUT}^2 \times D) \times \left(1 + \frac{1}{3} \times \left(\frac{\Delta i_L}{I_{OUT}}\right)^2\right) \times R_{DS\,(ON)} \quad (24)$$

If the inductor ripple current is fairly small, the conduction losses can be simplified to:

$$P_{COND} = I_{OUT}^2 \times R_{DS(ON)} \times D \quad (25)$$

Switching losses are also associated with the internal power switch. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node.

Switching Power Loss is calculated as follows:

$$P_{SWR} = 0.5 \times (V_{IN} \times I_{OUT} \times f_{SW} \times T_{RISE}) \quad (26)$$

$$P_{SWF} = 0.5 \times (V_{IN} \times I_{OUT} \times f_{SW} \times T_{FALL}) \quad (27)$$

$$P_{SW} = P_{SWR} + P_{SWF} \quad (28)$$

The power loss required for operation of the internal circuitry is given by:

$$P_Q = I_Q \times V_{IN} \quad (29)$$

I_Q is the quiescent operating current, and is typically around 3.2mA for the LMR10530X, and 4.3mA for the LMR10530Y.

An example of efficiency calculation for a typical application is shown in Table 1:

Table 1. Power Loss Tabulation

Conditions		Power loss	
V_{IN}	5V		
V_{OUT}	3.3V		
I_{OUT}	3.0A	P_{OUT}	9.9W
V_D	0.33V	P_{DIODE}	277mW
$R_{DS(ON)}$	56mΩ	P_{COND}	363mW
f_{SW}	1.5MHz		
T_{RISE}	10ns	P_{SW}	225mW
T_{FALL}	10ns		
IND_{DCR}	28mΩ	P_{IND}	252mW
I_Q	3.2mA	P_Q	16mW
η	89.7%		
D is calculated to be 0.72			

$$P_{LOSS} = \Sigma \left(P_{COND} + P_{SW} + P_Q + P_{IND} + P_{DIODE} \right) \quad (30)$$

$$P_{LOSS} = 1.133W \quad (31)$$

PCB LAYOUT CONSIDERATIONS

When planning layout there are a few things to consider to achieve a clean, regulated output. The most important consideration is the close coupling of the GND connections of the input capacitor Cin and the catch diode D1. These ground ends should be close to one another and be connected to the GND plane with at least two through-holes. Place these components as close to the IC as possible. The next consideration is the location of the GND connection of the output capacitor Co, which should be near the GND connections of C1 and D1. There should be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island. The signal ground SGND (pin 3) and power ground PGND (pin 6) should be tied together and connected to ground plane through vias.

The FB pin is a high impedance node and care should be taken to make the FB trace short to avoid noise pickup that causes inaccurate regulation. The feedback resistors should be placed as close as possible to the IC, with the GND of Rfbb placed as close as possible to the SGND of the IC. The V_{OUT} trace to Rfb1 should be routed away from the inductor and any other traces that are switching.

High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they should be as short and wide as possible. Radiated noise can be decreased by choosing a shielded inductor.

The remaining components should also be placed as close as possible to the IC. Please see Application Note AN-2280 SNVU192 for further considerations and the LMR10530 demo board as an example of a four-layer layout.

LMR10530X Design Example 1

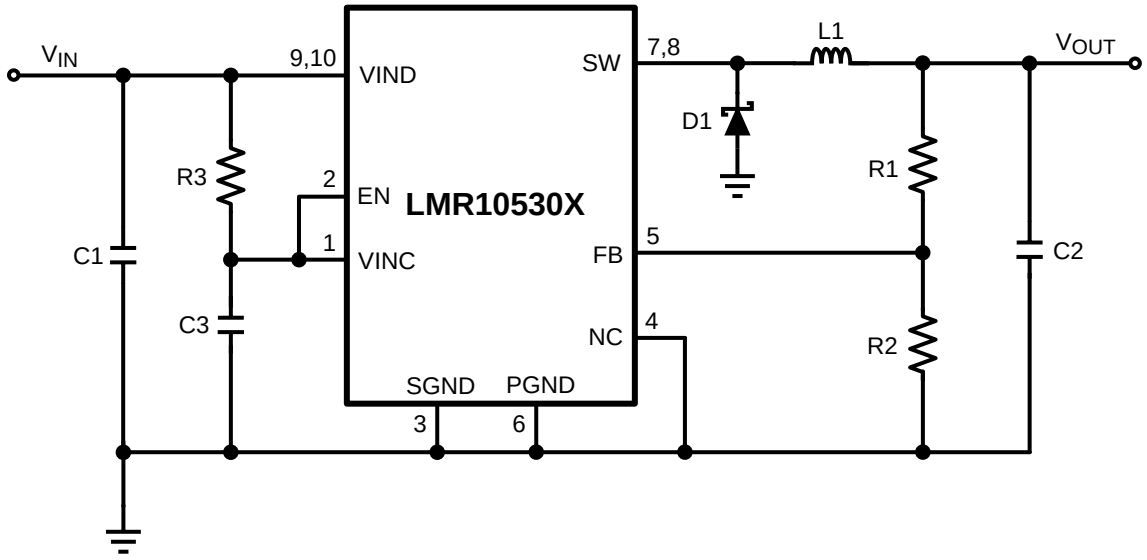


Figure 32. LMR10530X (1.5MHz): V_{IN} = 3.3V, Output = 1.2V/3.0A

Table 2. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	3.0A Buck Regulator	TI	LMR10530X
C1, Input Cap	22µF, 6.3V, X5R	TDK	C3216X5R0J226M
C2, Output Cap	47µF, 6.3V, X5R	TDK	C3216X5R0J476M
C3, Bypass Cap	0.22µF, 10V, X7R	Murata	GRM216R71A224KC01D
D1, Catch Diode	Schottky, 0.33V at 3A, V_R=30V	Toshiba	CMS01
L1	1.8µH, 3.6A	TDK	LTF5022T-1R8N3R6
R1	2.0kΩ, 1%	Vishay	CRCW08052K00FKEA
R2	2.0kΩ, 1%	Vishay	CRCW08052K00FKEA
R3	10Ω, 1%	Vishay	CRCW080510R0FKEA

LMR10530X Design Example 2

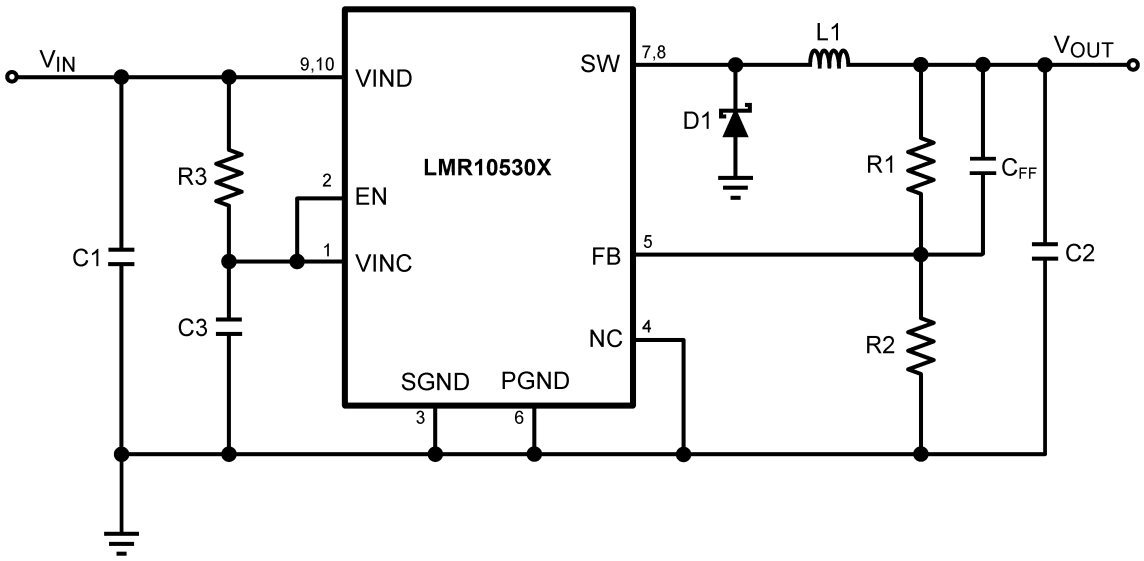


Figure 33. LMR10530X (1.5MHz): V_{IN} = 5V, Output = 3.3V/3.0A

Table 3. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	3.0A Buck Regulator	TI	LMR10530X
C1, Input Cap	22µF, 6.3V, X5R	TDK	C3216X5R0J226M
C2, Output Cap	47µF, 6.3V, X5R	TDK	C3216X5R0J476M
C3, Bypass Cap	0.22µF, 10V, X7R	Murata	GRM216R71A224KC01D
C_{FF}, Feed-forward Cap	47nF, 10V, X7R	AVX	0805ZC473JAZ2A
D1, Catch Diode	Schottky, 0.43V at 3A, V_R=30V	Vishay	SSA33L-E3/61T
L1	1.2µH, 4.2A	TDK	LTF5022T-1R2N4R2
R1	10.2kΩ, 1%	Vishay	CRCW080510K2FKEA
R2	2.26kΩ, 1%	Vishay	CRCW08052K26FKEA
R3	10Ω, 1%	Vishay	CRCW080510R0FKEA

LMR10530Y Design Example 3

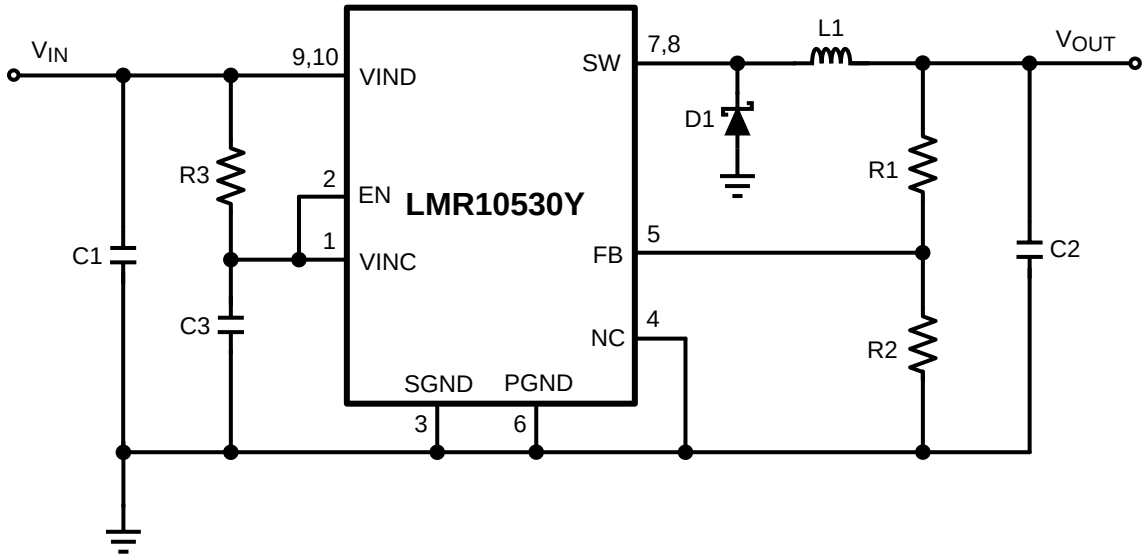


Figure 34. LMR10530Y (3MHz): V_{IN} = 3.3V, Output = 1.2V/3.0A

Table 4. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	3.0A Buck Regulator	TI	LMR10530Y
C1, Input Cap	22µF, 6.3V, X5R	TDK	C3216X5R0J226M
C2, Output Cap	47µF, 6.3V, X5R	TDK	C3216X5R0J476M
C3, Bypass Cap	0.22µF, 10V, X7R	Murata	GRM216R71A224KC01D
D1, Catch Diode	Schottky, 0.33V at 3A, V_R=30V	Toshiba	CMS01
L1	1.0µH, 4.0A	Taiyo Yuden	NP04SZB1R0N
R1	2.0kΩ, 1%	Vishay	CRCW08052K00FKEA
R2	2.0kΩ, 1%	Vishay	CRCW08052K00FKEA
R3	10Ω, 1%	Vishay	CRCW080510R0FKEA

LMR10530Y Design Example 4

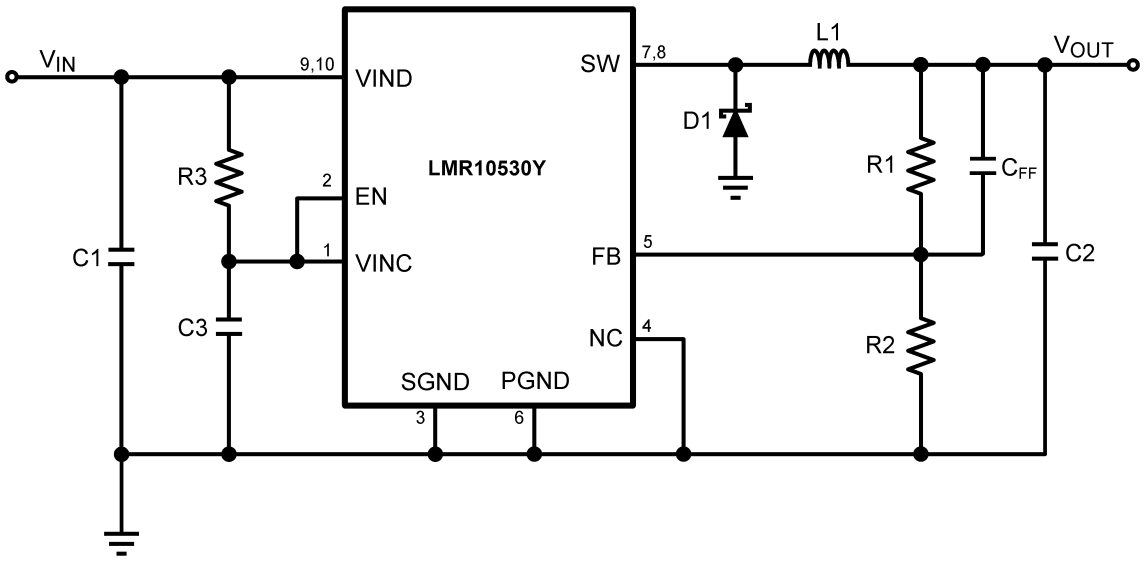


Figure 35. LMR10530Y (3MHz): V_{IN} = 5V, Output = 3.3V/3.0A

Table 5. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	3.0A Buck Regulator	TI	LMR10530Y
C1, Input Cap	22µF, 6.3V, X5R	TDK	C3216X5R0J226M
C2, Output Cap	47µF, 6.3V, X5R	TDK	C3216X5R0J476M
C3, Bypass Cap	0.22µF, 10V, X7R	Murata	GRM216R71A224KC01D
C_{FF}, Feed-forward Cap	47nF, 10V, X7R	AVX	0805ZC473JAZ2A
D1, Catch Diode	Schottky, 0.43V at 3A, V_R=30V	Vishay	SSA33L-E3/61T
L1	1.0µH, 4.0A	Taiyo Yuden	NP04SZB1R0N
R1	10.2kΩ, 1%	Vishay	CRCW080510K2FKEA
R2	2.26kΩ, 1%	Vishay	CRCW08052K26FKEA
R3	10Ω, 1%	Vishay	CRCW080510R0FKEA

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	24

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMR10530XSD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L287B	Samples
LMR10530XSDX/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L287B	Samples
LMR10530YSD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L286B	Samples
LMR10530YSDX/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L286B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

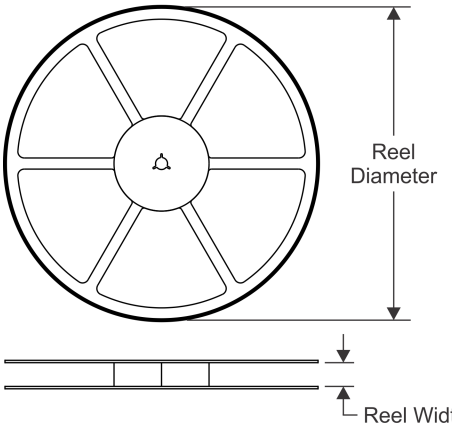
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

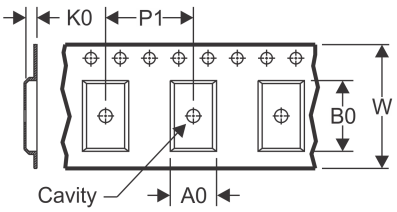
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

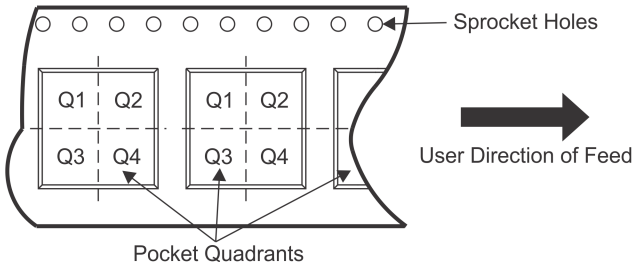


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

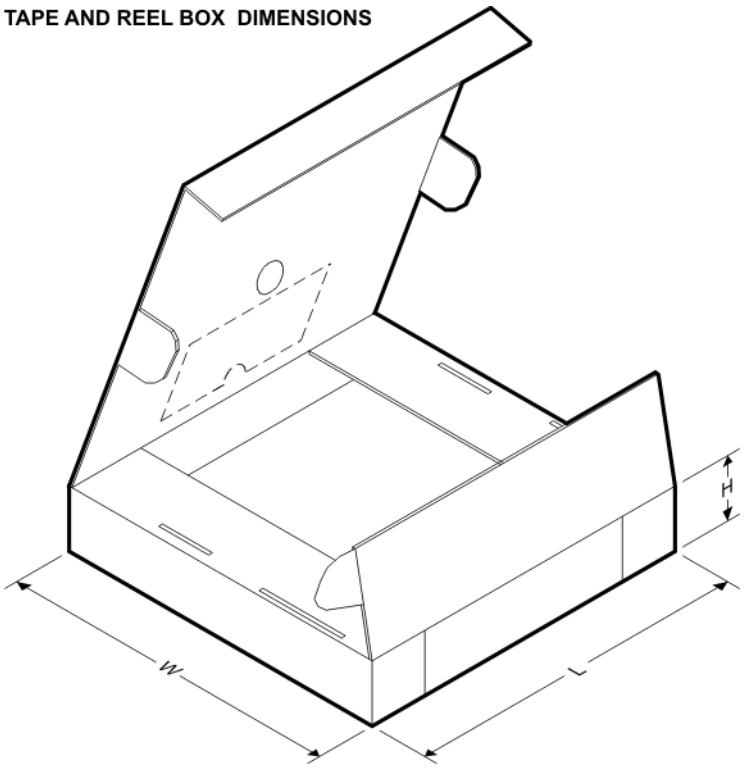
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR10530XSD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR10530XSDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR10530YSD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR10530YSDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

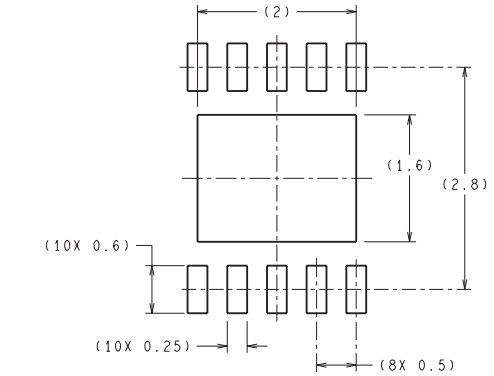
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

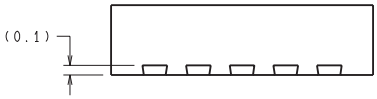
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR10530XSD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LMR10530XSDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0
LMR10530YSD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LMR10530YSDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

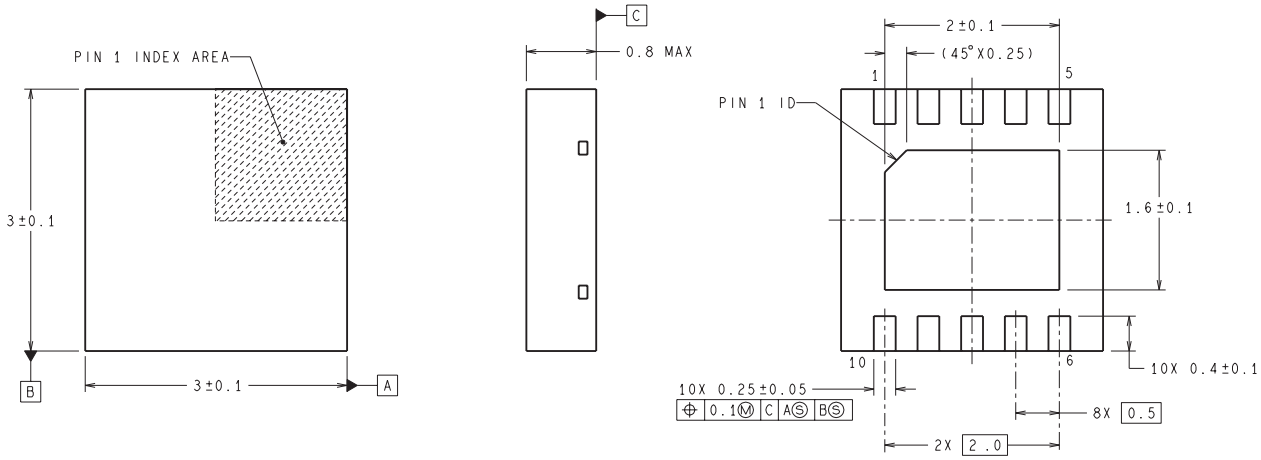
DSC0010A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





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