Using Thermal Calculation Tools for Analog Components

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ABSTRACT

This document provides general guidance on the use of tools and calculations for thermal estimates of component operating temperatures for analog devices. Of particular focus are components with direct thermal paths to the PCB, which is common for components which need a low thermal resistance to manage the dissipated power. This document provides practical considerations for estimation of operating temperatures while still in the design stages of the system. All device operating temperatures should be confirmed with measurements to ensure the maximum operating specs are met.

1   Component Thermal Classification

For the purposes of this discussion, electronic components will be classified into three categories with regard to their power dissipation and required thermal resistance. These are not rigid categories and are a function of several parameters such as package size, construction, materials, die size, and power dissipation profile. These categories can serve as a general guideline when considering the level of thermal analysis needed for a component during system design.

(a) The first category is referred to as "low power" components. These are generally components such as passives, logic devices, or other components that do not dissipate high levels of power during operation. Low power components generally do not require any thermal analysis and can be designed in to almost any system without concern of exceeding the maximum operating characteristics. There is no rigid definition of this category, but generally, if the temperature rise in an appropriate JEDEC thermal test environment, as calculated by the test coupon Theta-JA (θ_{JA}) multiplied by the power (θ_{JA} x Power) is less than 10°C, it could be considered low power. Depending on the component construction and application environment, the tolerance for low power could be as low as 100mW or less, or could reach as high as 500mW or even 1W (for example in systems with forced airflow). Ultimately, if there is any uncertainty, a component should be considered in the next category.

(b) The second category is referred to as "medium power" components. These are generally components which are dissipating enough power that their maximum operating temperatures could be exceeded, if care is not taken with good system and PCB design. These components have generally been designed to operate safely, provided that they are able to dissipate heat through a specific thermal path. For example, many medium power components are designed with a direct thermal path such as an exposed pad, which connects to a PCB pad with vias into a spreading plane. Medium power components require some thermal consideration during system design, and verification with measurements on the assembled system is essential. Because their heat dissipation paths are often carefully considered by the component supplier, medium power parts can often be analyzed during the system design phase using calculators or simplified modeling approaches, and then confirmed with measurements during the prototype phase. For these reasons, this document focuses particularly on methods to design for medium power devices, and particularly those using exposed pads to connect to the PCB thermal path. There is no rigid definition of this category, but generally components which would have a temperature rise of at least 10°C above the ambient temperature could be considered as medium power or possibly even in the next category. This temperature rise can be estimated by multiplying the appropriate JEDEC θ_{JA} by the power (θ_{JA} x Power), but this calculation should only be considered as preliminary and as an initial threshold for more thorough analysis. Some examples of components which are considered "medium power" would be those which have a high temperature rise above the ambient or PCB temperature, components which will operate in an environment with high ambient temperatures, or components which is in close proximity with other parts that contribute to the temperature rise of the PCB and overall system.

(c) The third category will be referred to as "high power" components. These are generally components which require careful and proactive system thermal design and validation to ensure maximum operating specifications are not exceeded. High power components often require specific thermal management solutions such as heat sinks, chassis conduction paths, or forced airflow. System designers are encouraged to perform detailed system analysis using modeling tools or test components for high power components, to ensure the optimal heat dissipation path is available in the system. There is no rigid definition of this category, but generally components which would have a high temperature rise above ambient and thus require a carefully designed thermal path (above and beyond traditional PCB layout best practices) could be considered as high power.

In summary, there are no rigid definitions or universally accepted guidelines for component thermal management, due to variations in the component construction, PCB construction and layout, and system environment. For the general category of "medium power" components which are designed to dissipate heat through a specific thermal path, it is often possible to use calculators or simplified approaches during the system design phase.

2   Exposed Pad Packages

Exposed pad packages are commonly used for medium power components. This is because they provide a low thermal resistance through the exposed pad to the PCB, and when the PCB is designed appropriately it is often sufficient to operate the components within the maximum operating conditions.

Exposed pad packages generally consist of an IC die sitting on a copper pad, where the copper pad is exposed on the outside surface of the component package. Some examples of exposed pad packages include HQFP (thermal QFP and variations such as TQFP and LQFP), HTSSOP (thermal TSSOP and variations such as SSOP and VSSOP), QFN (quad flat no-lead and variations such as SON), and older power packages such as TO or DDPAK families. Figure 1 illustrates some examples of these packages.
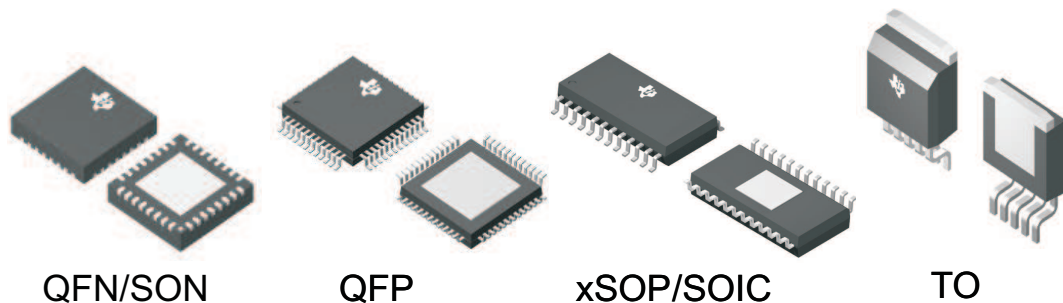

Figure 1. Examples of Exposed Pad Packages

The means of heat dissipation out of exposed pad packages (often referred to as the "thermal path") is illustrated in Figure 2. The heat is generated on the top of the IC die. The heat then flows down through the die, which is generally composed of silicon which is a strong thermal conductor. Then the heat flows through the die attach material, which is generally a thin layer of epoxy with moderate to poor thermal conductivity. The heat then flows through the die pad, which is generally a copper alloy and has very high thermal conductivity and also helps to spread the heat out. This overall thermal path enables thermal dissipation from the exposed die pad out into the PCB and system, with relatively low thermal resistance.
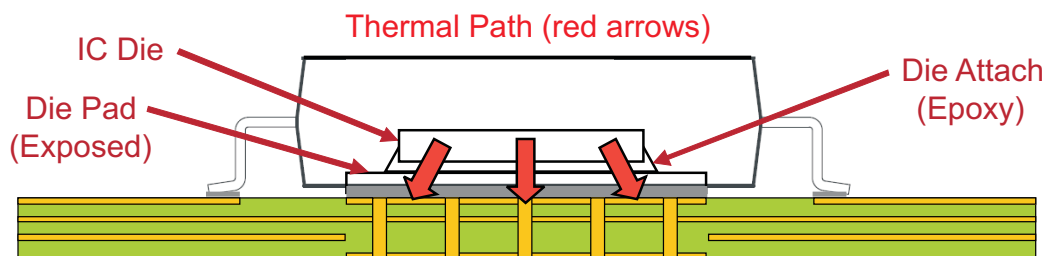

Figure 2. Exposed Pad Package Thermal Path

3 PCB Design

PCB design is essential for thermal management of medium and high power components. In many cases, PCB design is more consequential than the component or package characteristics themselves! For high power components, or components in particularly harsh systems, detailed system level thermal modeling or prototype measurements are often required. Medium power components are cooled primarily through the PCB thermal vias and copper planes. In this case, PCB design is the primary consideration for thermal management. As PCB thermal factors are reasonable to estimate, they can often be adequately addressed with good design practices, tools such as calculators or simplified modeling, and measurement confirmation on the final system.

Several key factors impact PCB design for medium power components in exposed pad packages These are covered in more detail in TI Application Note SLMA002. Additionally, design rules are included in the datasheet for all devices with an exposed pad. A short summary of the main factors are listed here and illustrated in Figure 3.

(a) Landing pad: the landing pad on the top of the PCB should be the same size or larger than the exposed pad of the component. The component should be soldered to the pad with reasonable coverage to ensure good heat conduction from the component to the PCB (more detail on soldering can be found in SLMA002). The outermost portions of the landing pad should be free from solder mask as these are the most important for spreading into the PCB.

(b) Spreading plane: there must be at least one Cu spreading plane in the PCB. This plane serves to conduct the heat from the small area of the component to a larger area in the PCB, where the heat is then dissipated through convection and radiation into the surrounding environment. As such, the plane must have sufficient thickness and area to provide adequate heat sinking for the component. Electrically, the plane is normally held at ground for exposed pad packages. As illustrated in Figure 2, the spreading plane may be located on the top layer and directly connected to the landing pad. This is often the case for packages such as TSSOP or SON. The spreading plane(s) may also be located on a buried layer(s) and connected to the vias. Buried spreading planes are commonly used with packages such as QFN or QFP.
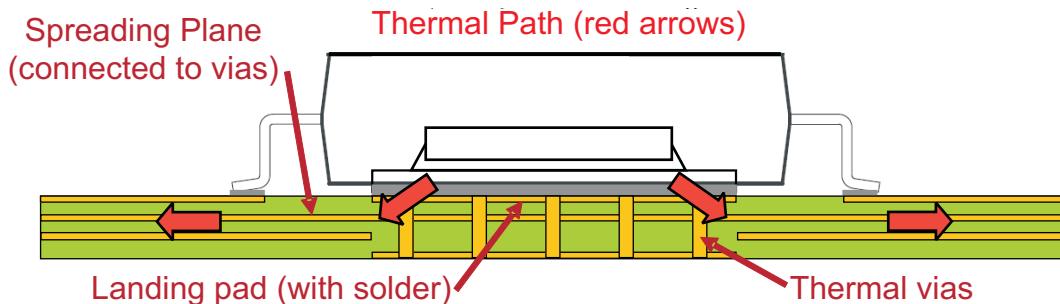

Figure 3. PCB Thermal Path

(c) Vias: When a buried spreading plane is employed, the landing pad should be connected by an array of vias to the buried plane to ensure good heat conduction from the exposed. Details of via designs can be found at SLMA002. A landing pad with insufficient vias to buried power and ground planes will not conduct sufficient heat from the package into the PCB spreading planes, and high temperatures may result

The spreading plane is of particular importance to the thermal performance of exposed pad packages and should be one of the primary considerations in PCB design. For adequate thermal management, it must have a specific area. The larger the spreading plane, the cooler the devices will run, so it should be as large as possible beyond the minimum area. Thermal analysis should be performed to ensure the plane meets the minimum area required to keep the junction temperature below the absolute maximum temperature. An example of a graph which illustrates the impact of spreading plane area on junction temperature for an example device and PCB stack-ups is shown in Figure 4. More precise definitions of Enhanced and Minimum Thermal PCBs are described in later sections. The area of the spreading plane (assumed to be continuous, having no breaks) is shown on the x-axis, and the resulting temperature is shown on the y-axis. It can be noted that below a certain size, the temperature rises dramatically as there is little copper area available to cool the component. Similarly, for a copper area larger than a certain size, the impact on the temperature diminishes significantly as the heat is sufficiently spread out .
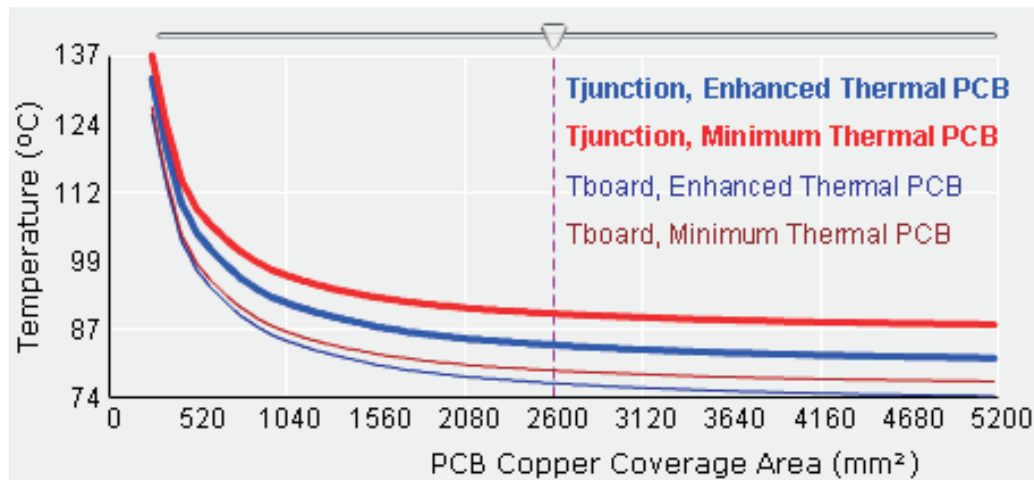
Figure 4. Example Graph Showing Junction Temperature as a Function of Spreading Plane Area for the TAS5701PAP Device at 0.5W with 65°C Ambient Temperature

4   System Design Using Spreading Plane Estimates

A good system level thermal design and analysis must account for the primary factors in the system which would influence the flow of heat from the component out to the surrounding environment. It is often not practical to analyze these factors in the full level of detail (through modeling or prototyping) due to restrictions of time, cost, availability of tools or expertise, or resolution of fine geometric or thermal details. During system design, thermal estimates are often made to predict final thermal performance. These estimates can include explicitly using simplified tools or methods, implicitly using rules or thumb, basing decisions on historical success, planning for large margins of error, or other methods of varying complexity.

For low or medium power components using exposed pad packaging, where the board temperature cannot be measured during the design stages, there are several reasonable methods of simplification which can be used. Several of these are described here:

(a) PCB layout is an important thermal design factor. The presence of the landing pad and vias, and the design and size of the spreading plane are important for heat spreading to eventually transfer to the surrounding environment. The variability in a real system is often due to PCB stackup (Number of layers, thickness of Cu foil and plating, and plane design). Systems which plan to use medium power components must have at least one spreading plane. This plane must be reasonably continuous (minimal breaks in the direction of heat flow) in the area that is considered for spreading. The minimum thickness of a spreading plane in a typical PCB is ½ Oz. Often PCB's are enhanced by using planes that are 1 Oz, or in rare occasions even thicker. The presence of thicker or additional thermal spreading planes can give further improvement, but the effect can be diminishing. For medium power components with a reasonably continuous spreading plane, rather than analyzing the detailed plane layout, it is a reasonable simplification to use a single continuous spreading plane of ½ to 1 Oz.

(b) Other components on the PCB can have a significant thermal effect on the component of interest, depending on their design, thermal dissipation, and proximity. Every system and every component is different, so it is nearly impossible to analyze in full detail the full list of components on the PCB, and simplifications must be made. The first simplification which is commonly taken is to ignore components such as passives which have very low dissipation, and to focus only on components which have more than 50-500mW of dissipation (depending on the system and accuracy needed). The next level of simplification which is effective for focusing on a specific component is to use symmetry (or adiabatic) lines which do not allow heat flow across them, so that the interaction between components is effectively negated. Medium power components often have a spreading plane which is effectively dedicated for them, so it is reasonable to draw symmetry lines around the spreading plane. For components which share a spreading plane, it is reasonable to divide the total spreading plane area by the number of components (or a ratio of their power dissipation), to derive an effective Cu spreading plane area to use for calculations.

(c) The design of the enclosure in which the PCB sits is an important contributor to the effectiveness of the convection of the heat from the PCB to the surrounding air. Medium power components often do not have forced airflow, and are cooled by natural convection. The effectiveness of natural convection cooling is often dictated by the freedom of air to circulate within the enclosure. One important factor is the orientation with respect to the gravitational direction, as a vertically-oriented PCB can create a strong "chimney effect" which aids in the effectiveness of the convection. Unfortunately, it is rarely possible to ensure that a system stays oriented vertically during its use, so a horizontal orientation is the conservative simplification to use. Another important contributor is the open space above or below the PCB where the air to circulates. The rule is that if the space above and below the board is less than 6mm and there is no fan circulating the air, there is no convection. This case is not considered by the simple board level junction temperature estimator.

In summary, analysis of many medium power components during the design stage can be simplified using assumptions of a ½ to 1 Oz continuous spreading layer in the PCB, which uses symmetry lines for heat flow to focus on a particular component, using typical convection calculation methods if the available space above the PCB is greater than 6mm.

5   Calculations using Board Temperature

The best and most accurate method to estimate the component temperature (often called operating temperature or junction temperature) is to use the board temperature. If the board temperature and component power dissipation can be estimated, then the component temperature can be estimated using the equation:

$$T_J = T_B + Pdiss \times \Psi_{JB} \tag{1}$$

Where:

- T_J = Junction temperature of the device
- T_B = Board temperature (1mm from device, as defined by JESD51-2)
- Pdiss = Power dissipated by the device
- Ψ_{JB} = Junction to board thermal parameter (as defined by JESD51-2 or customized for a lesser PCB stackup)

In this case, the calculation can be made independently of the PCB layout and is much simpler, provided that the board temperature used can be maintained in the subsequent system environment. It should also be noted that a PCB with a minimal thermal stackup (such as a single ½ Oz plane for heat spreading) will have a higher spreading resistance under the package, which can raise the Ψ_{JB} value up to 25% higher than the JEDEC value.

6   TI's PCB Thermal Calculator

To support the growing needs for quick and simplified analysis during the system design stage of medium power components which use exposed pad packaging, TI has used simplifications like those described in Section 4 to create a calculator. This calculator is available at www.ti.com/pcbthermalcalc. This calculator may be used for many of TI's components, to generate a quick estimate of the expected junction temperature based on the Cu spreading area on the PCB.

Note that this calculator is based on detailed modeling and measurements under specific conditions, so care must be taken to ensure that the simplifications made are appropriate to the system of interest. These simplifications are described in Section 4, and the details of the data used for TI's calculator will be described in this section. The modeling approach used in TI's PCB Thermal Calculator are based on measured data considering 2 packages on 3 PCB designs with 2 stackups, including 3 of the 4 interactions, for a total of 9 sets of data. The two packages included were the 48PHP (HTQFP package requiring a buried spreading plane on the PCB) and the 56DCA (HTSSOP package allowing top spreading plane on the PCB). The 3 PCB designs include Cu spreading areas of 25 x 25mm, 40 x 40mm, and 74 x 74mm, as illustrated in Figure 5 and Figure 6. The two stack-ups include one with a thin spreading plane of ½ Oz (measured at 17μm) and a thick spreading plane based on plating and measured at 62μm to 73μm.
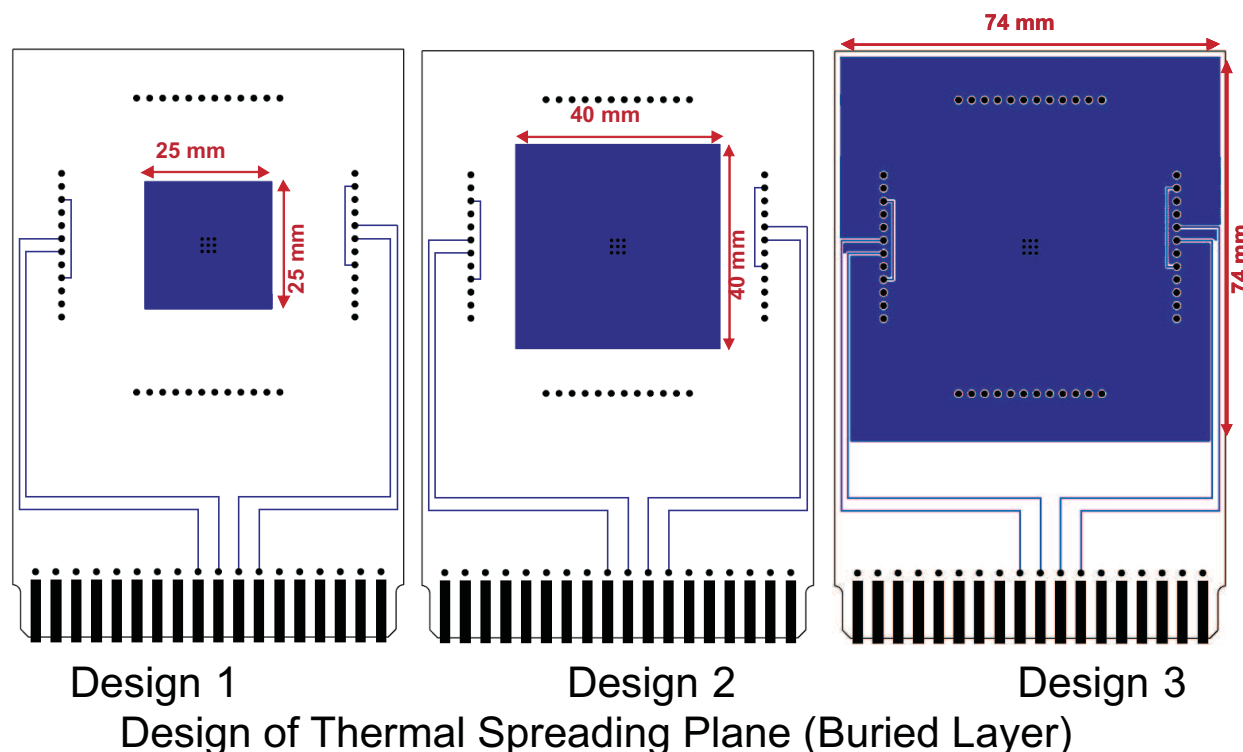
Figure 5. PCB Designs for Thermal Measurements of HTQFP Package with Buried Spreading Plane
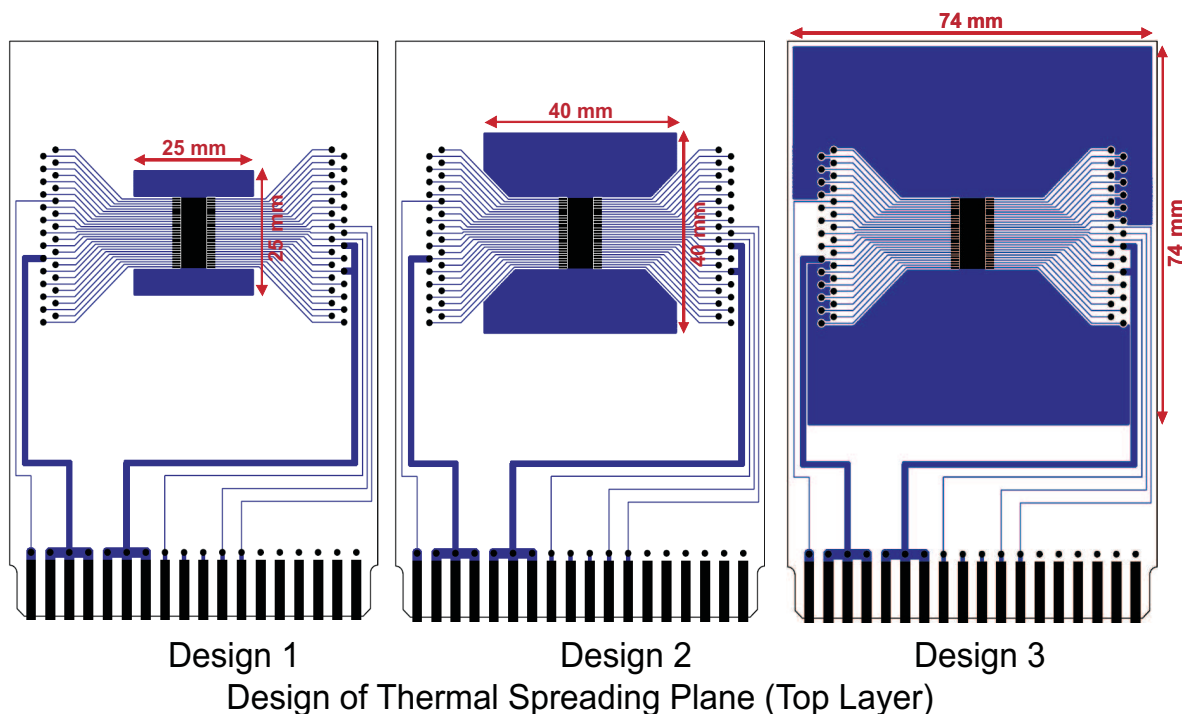

Figure 6. PCB Designs for Thermal Measurements of HTSSOP Package with Top Layer Spreading Plane

The measured data was collected using a K-factor thermal test die in a still air enclosure, using the test methods defined in JESD 51-1, 51-2 and 51-4. Detailed models were then run to correlate specifically to the measured data. Examples of the detailed models are shown in Figure 7, and the correlation of the

modeled to measured data is shown in Table 1. All of the modeling conditions correlated within 10% of measured data across the entire range of packages, spreading planes, and considering part to part and measurement to measurement variation. It must be noted that the spreader plane thicknesses considered in TI's calculator do not exactly match the thicknesses measured in PCBs used for thermal measurements. Even though the goal was to match the PCB constructions used in calculator and measurements, lack of precise plating thickness control lead to different final spreader plane thickness for the outer layers. Such deviations are not uncommon due to PCB manufacturing technology, which involves plating to form vias, which also plates copper over the outer exposed copper foils. Nevertheless, the thicknesses considered in calculator are within the 17µm and 73µm range found in PCBs used for measurements (they are interpolating, not extrapolating). The modeling approach was kept same for all the measured cases and was calibrated for these differences between measured geometry and calculator conditions. The error was within 10% for all cases, which is well within typical error ranges for thermal measurements and modeling.
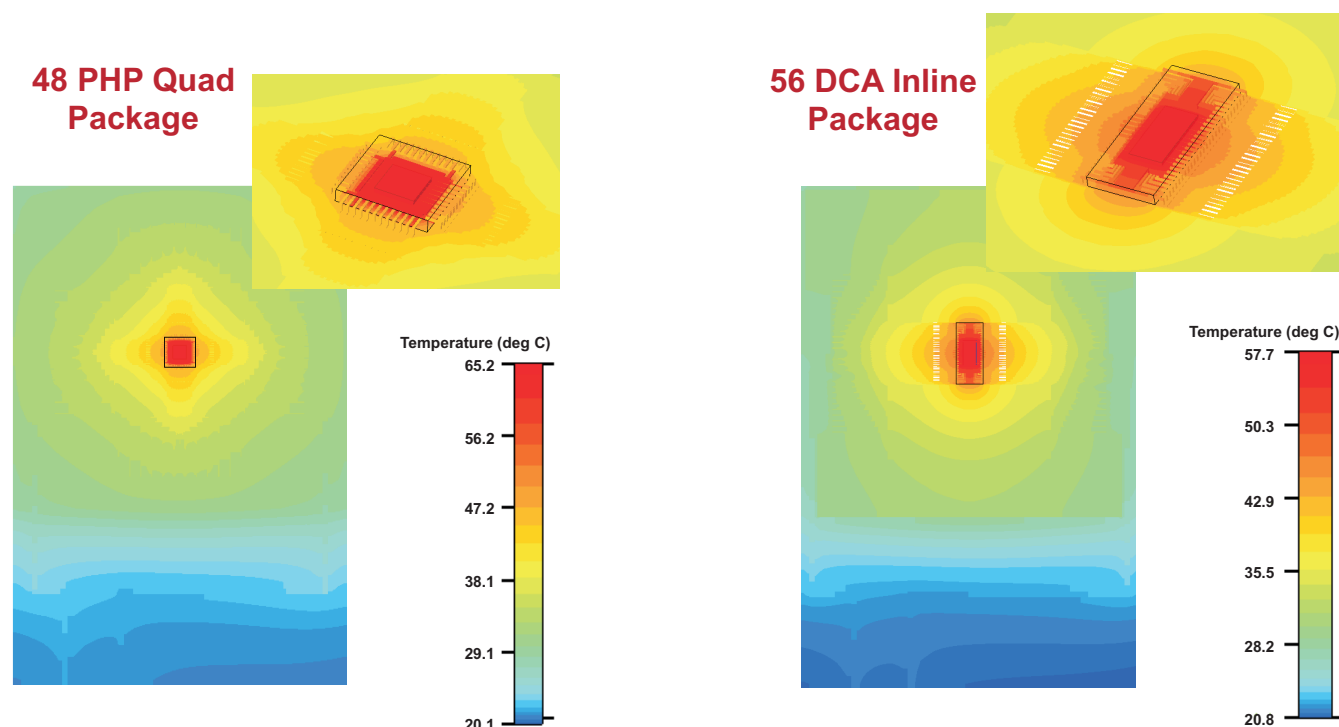
Figure 7. Examples of Detailed Models for Correlation to Measured Data

Table 1. Summary of Modeled and Measured Data

Package Type	Spreader Plane Thickness	Spreader Plane Size (mm)	θ_{JA}			θ_{JB}		
			Measured Average (C/W)	Model Prediction (C/W)	Deviation (%)	Measured Average (C/W)	Model Prediction (C/W)	Deviation (%)
48PHP	17 µm	25 x 25	51.5	52.8	2.6	17.1	18.5	8.1
		40 x 40	46.9	48.2	2.6	17.3	18.3	5.8
		74 x 74	43.9	44.7	1.9	17.3	18.4	6.5
	62 µm	25 x 25	40.5	44.0	8.8	13.1	14.3	9.7
		40 x 40	34.7	36.4	4.9	12.7	12.8	0.9
		74 x 74	31.7	29.9	-5.5	13.7	12.6	-8.4
56DCA	73 µm	25 x 25	39.5	41.9	6.2	9.9	10.8	8.9
		40 x 40	34.4	34.6	0.6	10.1	10.3	2.2
		74 x 74	30.3	29.0	-4.2	10.5	10.3	-2.2

This section provides a summary of modeling used to generate actual calculator data, the interpolation approach, and validation cases.

(a) The TI PCB Thermal Calculator estimates junction and board temperatures for devices using a thermal resistance network from junction to ambient. For the user-selected device, thermal resistances in the network are interpolated from pre-generated resistance data on different package sizes and exposed pad sizes. The thermal resistance data is generated from CFD simulations using commercially available thermal modeling software. Specific details on the simplified model are shown in Figure 8 and Figure 9. For exposed pad packages, the primary heat flow path is through the exposed pad itself. For general applicability, the package model ignores the variations in leadframe geometries which are found in customized designs for real devices. PCB traces on the top plane are treated as patches with orthotropic thermal conductivity in the in-plane direction. In the case of quad packages, thermal vias are modeled as an orthotropic block with effective properties. This simplifies parametric simulations needed for thermal resistance data generation. System details and layout of the metal stack-up in PCBs is summarized through Figure 8, Figure 9, and Table 2. PCB constructions are based on recommendations as indicated in TI Applications Note SLMA002 for thermal design of spreader plane and vias.
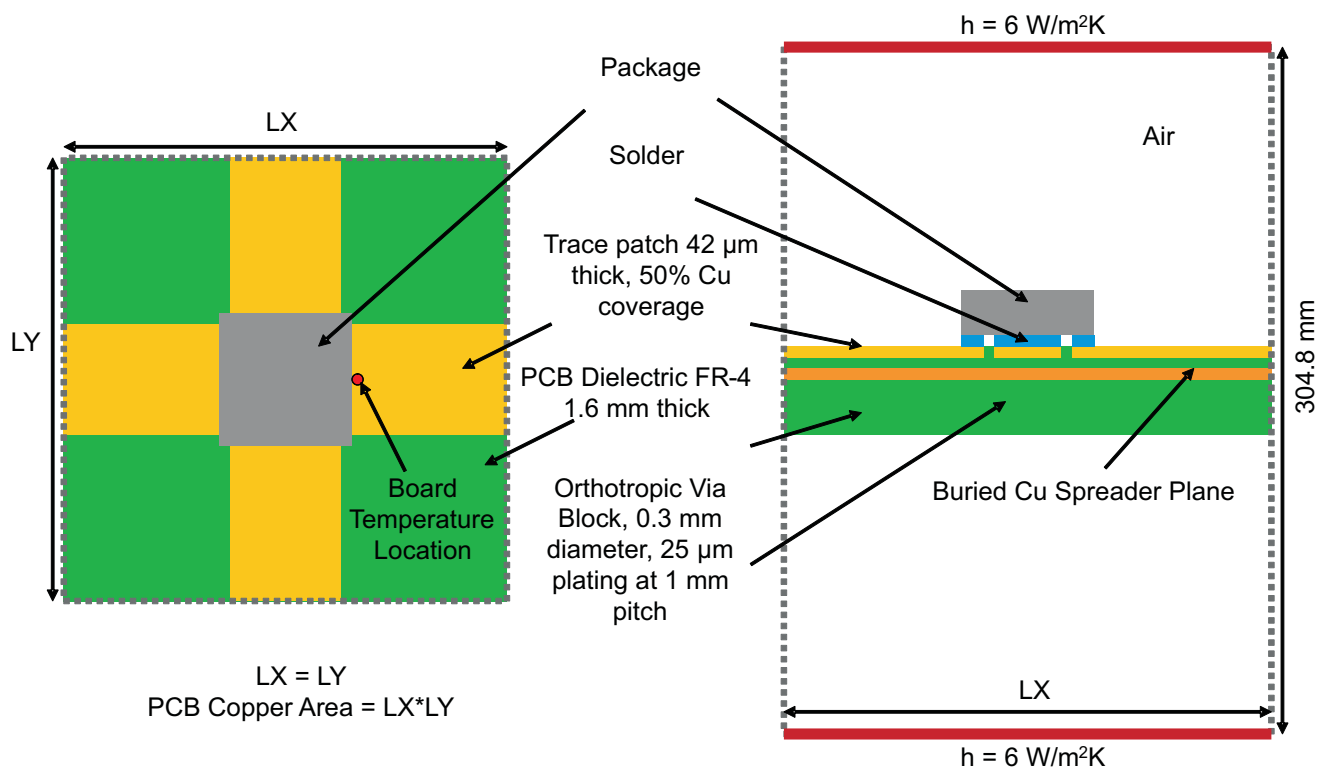
Figure 8. System Model Details for Quad Packages
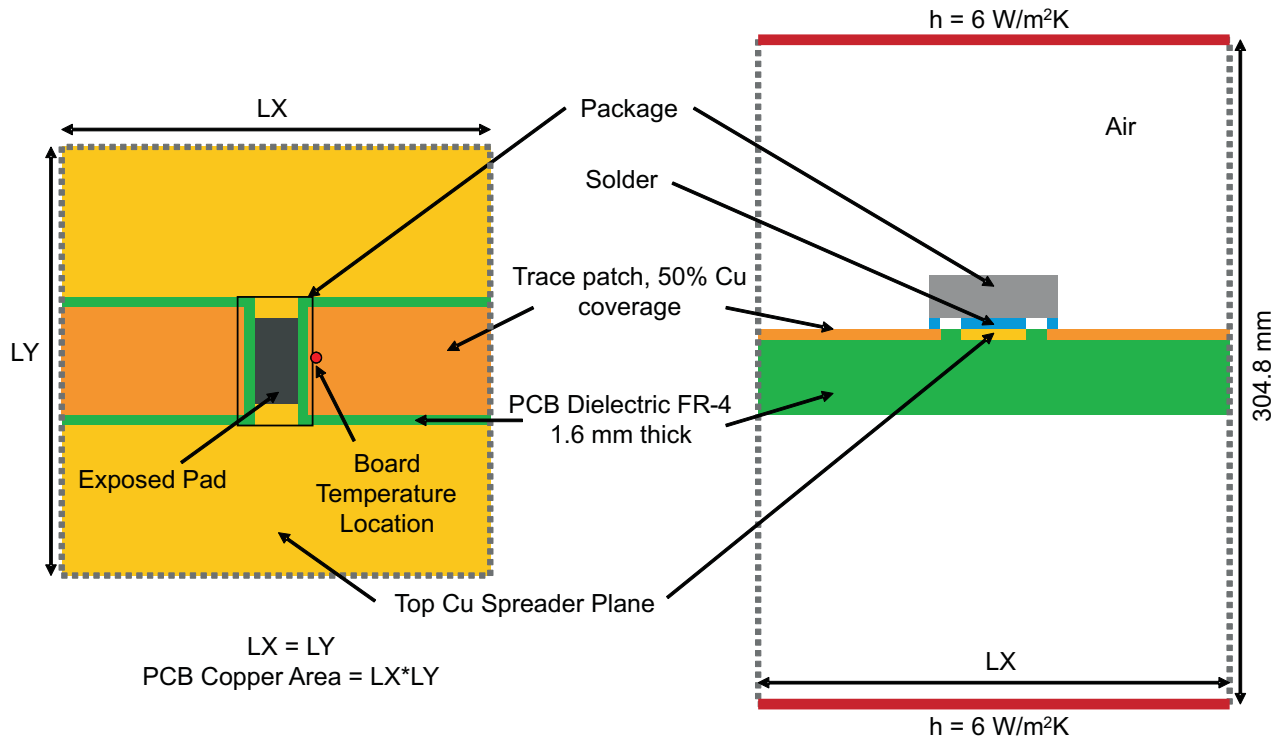
Figure 9. System Model Details for Inline Packages

Table 2. PCB Construction for Quad and Inline Packages

PCB Feature	Quad Packages		Inline Packages	
	Minimum Thermal PCB	**EnhancedThermal PCB**	**MinimumThermal PCB**	**EnhancedThermal PCB**
Spreading Plane	17 µm thick 1st Buried plane	35 µm thick 1st Buried plane	42 µm thick top plane (1/2 Oz + 25 µm plating)	60 µm thick top plane (1 Oz + 25 µm plating)
Trace Patch	42 µm top plane at 50% Cu Coverage	42 µm top plane at 50% Cu Coverage	42 µm top plane at 50% Cu Coverage	60 µm top plane at 50% Cu Coverage
Thermal Vias	To spreader plane	To spreader plane	None	None

(b) The calculator uses the resistance network shown in Figure 10 to generate curves for temperature rise. Heat transfer from an exposed pad package can be divided to flow through three paths: a) bottom of the package through the PCB to ambient air, b) top of the package to ambient air, and c) four sides of the package to the ambient air. Thermal resistances for these paths are extracted from more than a thousand CFD simulations with package and PCB copper area variations. For the user-selected device, each of θ_{TOP}, θ_{SIDE}, θ_{CA} thermal resistances are interpolated from the extracted thermal resistance data. θ_{CA} is in turn calculated by summing the Case-to-Board and Board-to-Ambient thermal resistance, where the latter depends on the PCB copper spreading area. Once these resistances are calculated, the Junction-to-Ambient thermal resistance θ_{JA} and junction temperature T_J is calculated using the following analysis for thermal resistances in parallel:

$$\frac{1}{\theta_{JA}} = \frac{1}{\theta_{JC,Bottom} + \theta_{CA}} + \frac{1}{\theta_{TOP}} + \frac{1}{\theta_{SIDE}}$$

$$\boldsymbol{T_J = \theta_{JA} \times P_{diss} + T_A}$$

(2)

Board temperature can be estimated using thermal characterization parameter θ_{JB} as follows:

$T_B = T_J - \Psi_{JB} \times Pdiss$ (3)

where: θ_{JB} is interpolated from extracted thermal characterization parameter data and device specific Junction-to-Case thermal resistance $\theta_{JC,Bottom}$.
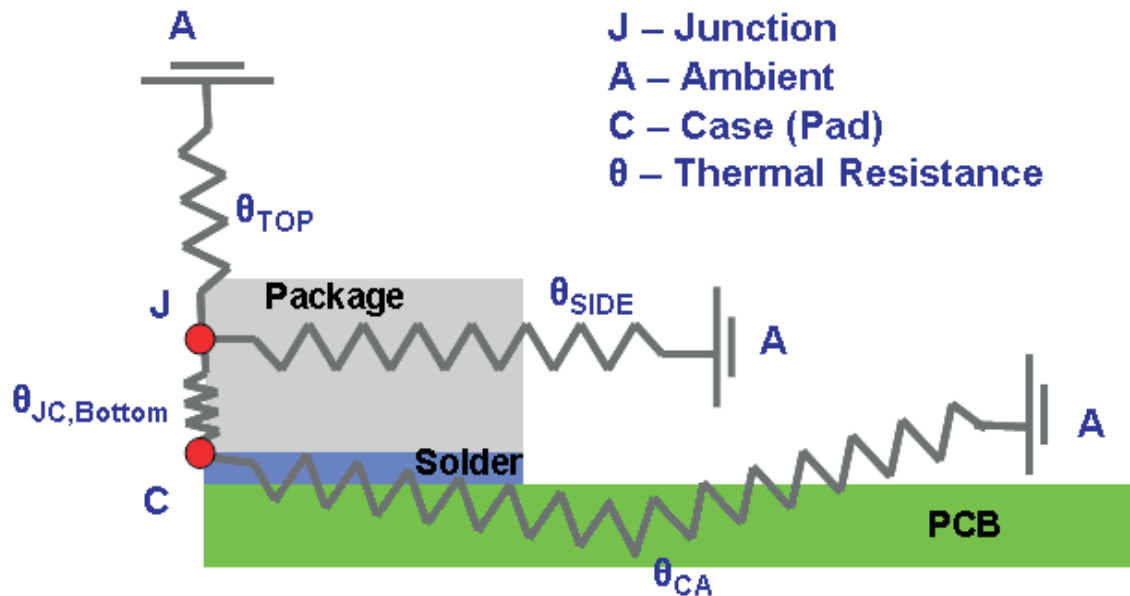
Figure 10. Schematic of Thermal Resistance Network

The interpolation approach was additionally validated with detailed models on packages not used in generating thermal resistance data. Validation was performed for two different package sizes for each of the Quad and Inline categories. As a further challenge, internal package features such as die size and pad size are varied to result in a wide range of $\theta_{JC,Bottom}$ values. The validation is summarized in Figure 11 for Quad and Figure 12 for Inline packages. The interpolation approach predicts thermal resistance well for both Enhanced Thermal and Minimum Thermal PCBs.
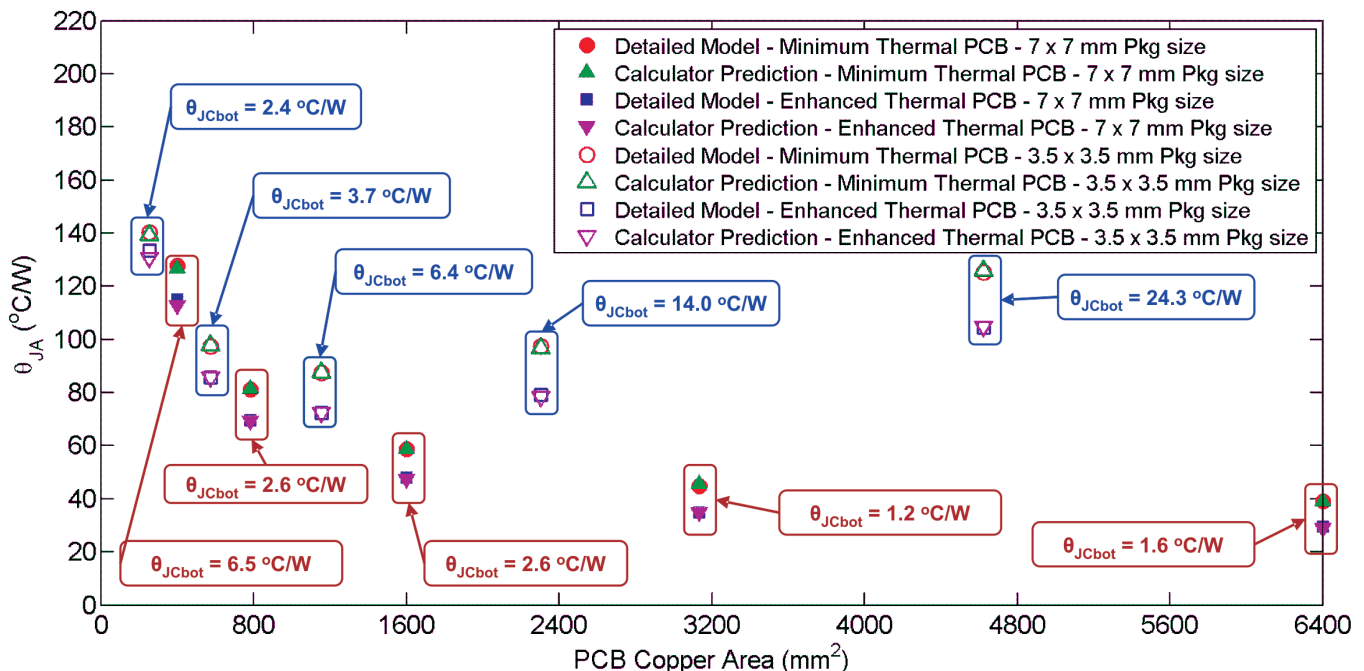
Figure 11. Validation of Interpolation Approach for Quad Packages
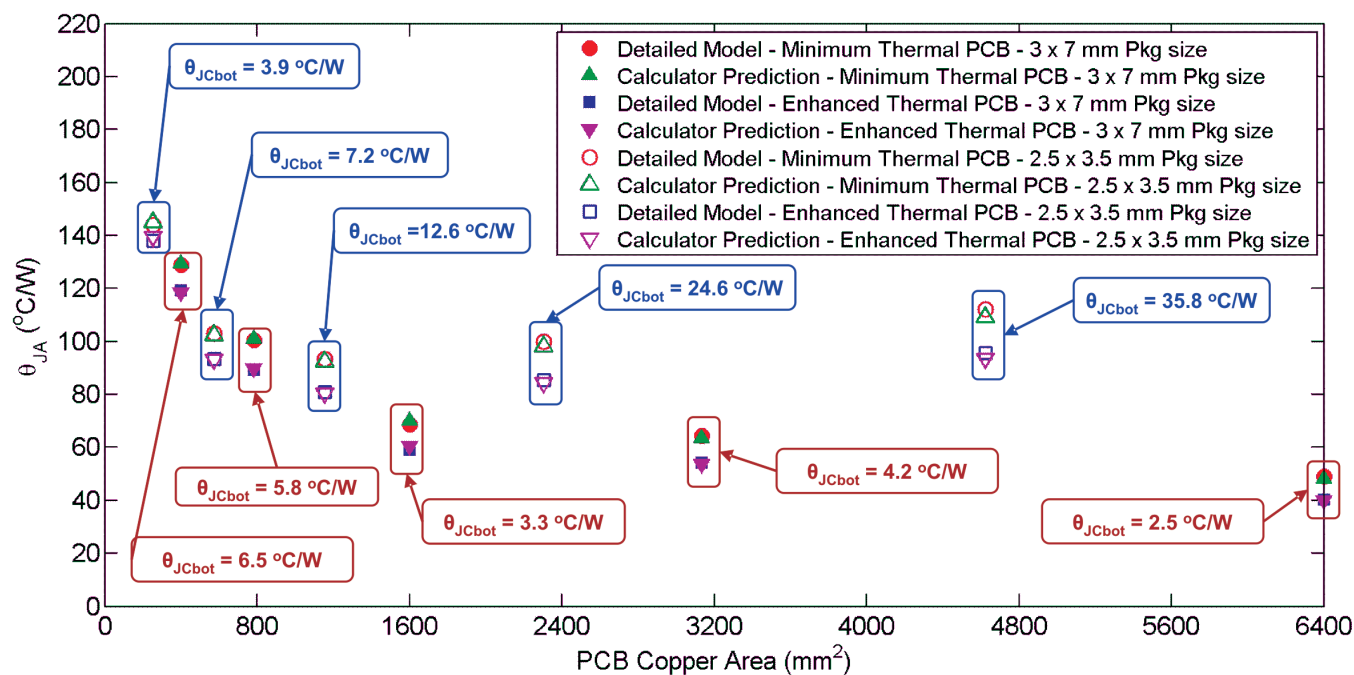
Figure 12. Validation of Interpolation Approach for Inline Packages

(c) As an example of calculator usage, Figure 13 shows the output curves from the calculator for TPS74201RGWR device in a 5 x 5 mm Quad package with $\theta_{JC,Bottom}$ of 2.4°C/W . In this example, the user inputs a power dissipation value of 1 W with a 50°C ambient air temperature. Upon clicking the Calculate button, two curves are plotted in the window for each type of PCB. The curves show the junction temperature and board temperature as a function of PCB copper coverage area. Larger copper area leads to lower temperatures.
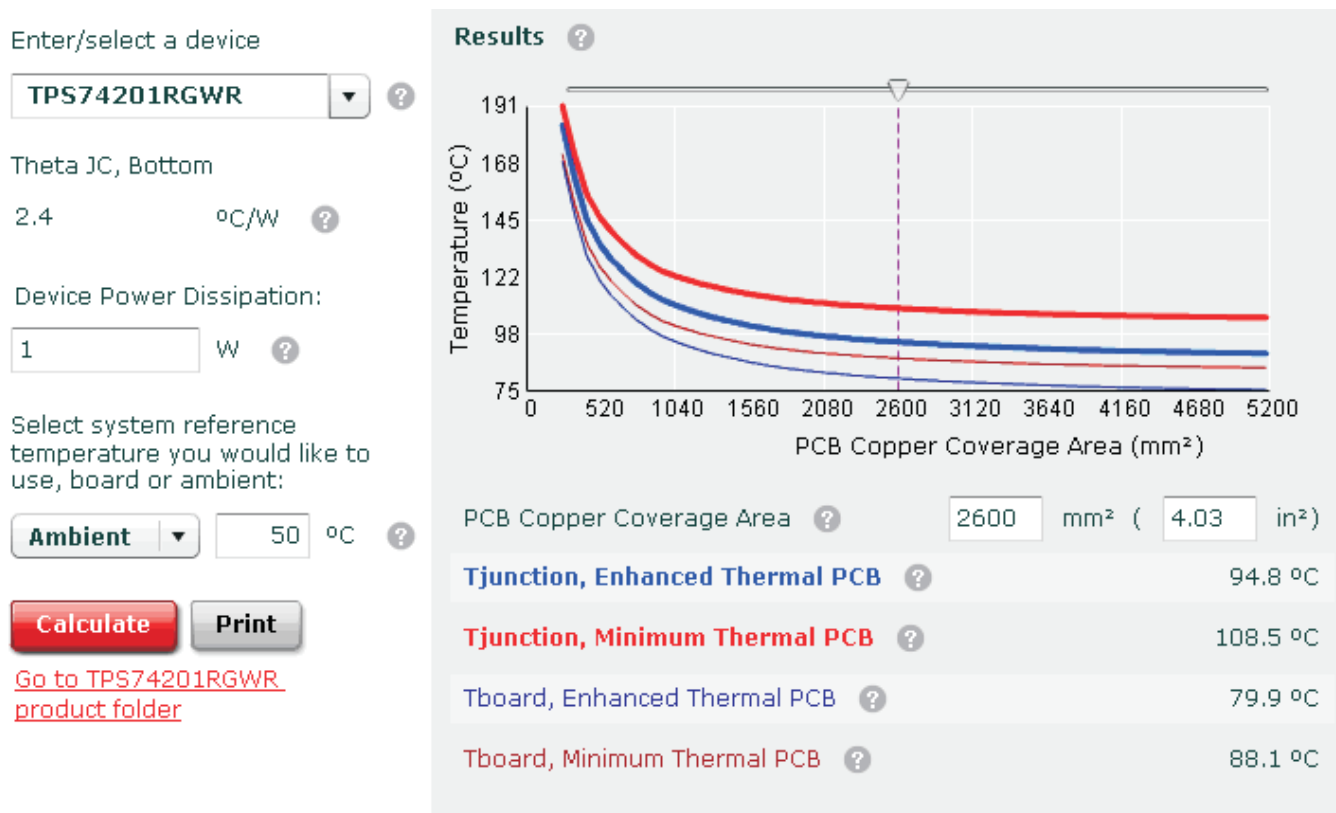
Figure 13. TI PCB Thermal Calculator Example

The TI PCB Thermal Calculator also includes the θ_{JB} values for the components (including values for Enhanced and Minimum Thermal PCB stackup), and as an output it provides the board temperature based on spreading area. It also allows the user to use board temperature as a reference and will estimate the junction temperature for each of the PCB stackup configurations.

7 Summary

Components can generally be classified into low power, medium power, and high power categories, although it is difficult to make a precise definition. Medium power components with an exposed pad can be cooled to below the specified maximum junction temperature by appropriate design of PCB spreader planes and thermal vias, and availability of air for natural convection cooling (free-air). Temperature rise for these components is a strong function of PCB construction, such as spreader plane area, thickness, and number of vias, in addition to component thermal characteristics. TI's PCB Thermal Calculator can help estimate a first-pass spreader plane area required to ensure that the temperature rise is below the maximum allowable device operating temperature. Predictions are provided for two types of PCBs (Minimum and Enhanced Thermal Capability). The PCB construction described in the previous sections must be compared with user's PCB and appropriate decision must be made. For example, if the user PCB's top spreader plane thickness is larger than 60μm for an inline package, it is expected that his temperature rise would be smaller than that predicted by the calculator for Enhanced Thermal PCB. Care must be taken in defining the available copper spreader area when there are multiple medium power components using the same spreader plane. It must be noted that the intent of the calculator is to reduce cycle time for design and development, and is not a replacement for detailed system-level CFD analysis using commercial software. Final design should always be verified through careful measurements against the maximum operating conditions as specified in the device data sheet.

8 Referenced Documents

http://www.ti.com/lit/pdf/SLMA002