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# LDO Thermal Calculations

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## Abstract

Low Dropout Regulators in present is the cheapest solution for precise voltage source with a few external components. However, the main disadvantage is loss conversion producing significant heat. Therefore proper thermal design is a key for good LDO performance in real applications.



# Agenda

- Thermal parameters standards, terminology and definitions
- Suitable packages for good thermal performance
- Thermal Calculators for LDOs
- Thermal Simulations Used in Silicon Design Phase



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# Thermal Parameters Standards, Terminology and Definitions



# Standards

- JEDEC specifications:
  - Find information related to  $\theta$  and  $\Psi$  parameters definitions and other useful information at website: [www.jedec.org](http://www.jedec.org) in “General Folder” click on “Free Standards” and in “Search by document number:” text field write “JESD51”
  - Glossary of Thermal Measurement Terms and Definitions (JESD51-13)



# Thermal to Electrical Analogy Used

Electrical		Thermal
Voltage (V)	↔	Temperature Difference (°C)
Current (A)	↔	Dissipated Power (W)
Resistance (Ω)	↔	Thermal Resistance (°C/W)

$$I_{R_{XY}} = \frac{V_{XY}}{R_{XY}}$$

$$P_D = \frac{T_X - T_Y}{\theta_{XY}}$$



# $\theta$ (Theta) - Thermal Resistance

$\theta_{XY}$  - Thermal Resistance between X and Y points specifies:

- The amount of heat that flows from point X to point Y if the temperatures at X and Y points are known (connected by the thermal resistance). The path the heat flows is known and it is completely determined by the resistance.

In general: 
$$P_D = \frac{T_X - T_Y}{\theta_{XY}} \quad \left( W = \frac{^{\circ}\text{C}}{^{\circ}\text{C}/\text{W}} \right)$$

Examples: 
$$P_D = \frac{T_{J\max} - T_A}{\theta_{JA}}$$

Calculation of Power Dissipation for given Maximum Junction Temperature and Ambient Temperature. Thermal Resistance is specified for particular application conditions.

- The temperature at point X if the temperature at point Y and the amount of heat are known. The path the heat flows is known and it is completely determined by the resistance.

In general: 
$$T_X = \theta_{XY} \cdot P_D + T_Y \quad ( ^{\circ}\text{C} = ^{\circ}\text{C}/\text{W} \cdot \text{W} + ^{\circ}\text{C} )$$

Examples: 
$$T_J = \theta_{JC} \cdot P_D + T_C$$

Calculation of Junction Temperature for given Power Dissipation and Case Temperature (i.e. Tab temperature for D2PAK). Thermal Resistance is specified for particular package. (Important: almost all heat flows through the Tab)

# $\Psi$ (Psi) - Thermal Characterization Parameter

$\Psi_{XY}$  - Thermal Characterization Parameter between X and Y points specifies:

- The temperature difference between point X to point Y if the total heat is known. The heat flowing along the specific path point X to point Y is NOT known.
- This parameter typically serves for estimation of Junction temperature ( $T_J$ ) at known total dissipated power ( $P_D$ ) inside the package when a temperature is measured at package perimeter (Lead, Exposed Pad, Board, etc.)

In general:  $T_X = \Psi_{XY} \cdot P_D + T_Y \quad (^\circ\text{C} = ^\circ\text{C}/\text{W} \cdot \text{W} + ^\circ\text{C})$

Examples:  $T_J = \Psi_{JLn} \cdot P_D + T_{Ln}$

Junction Temperature estimation by measuring  $n^{\text{th}}$  Lead (Pin) Temperature (SO, DFN, etc.)

$$T_J = \Psi_{JB} \cdot P_D + T_B$$

Junction Temperature estimation by measuring Board (Pad) Temperature (SO with Exposed Pad, DFN, etc.)





# Thermal Parameters in Datasheet (NCV4269)

**$T_{Jmax}$**

**MAXIMUM RATINGS** ( $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ )

Parameter	Symbol	Min	Max	Unit
Input to Regulator	$V_I$ $I_I$	-40 Internally Limited	45 Internally Limited	V
Input Transient to Regulator	$V_I$	-	60	V
Sense Input	$V_{SI}$ $I_{SI}$	-40 -1	45 1	V mA
Reset Threshold Adjust	$V_{RADJ}$ $I_{RADJ}$	-0.3 -10	7 10	V mA
Reset Delay	$V_D$ $I_D$	-0.3 Internally Limited	7 Internally Limited	V
Ground	$I_q$	50	-	mA
Reset Output	$V_{RO}$ $I_{RO}$	-0.3 Internally Limited	7 Internally Limited	V
Sense Output	$V_{SO}$ $I_{SO}$	-0.3 Internally Limited	7 Internally Limited	V
Regulated Output	$V_Q$ $I_Q$	-0.5 -10	7.0 -	V mA
Junction Temperature Storage Temperature	$T_J$ $T_{STG}$	- -50	150 150	$^{\circ}\text{C}$ $^{\circ}\text{C}$
Input Voltage Operating Range Junction Temperature Operating Range	$V_I$ $T_J$	- -40	45 150	V $^{\circ}\text{C}$

# Thermal Parameters in Datasheet (NCV4269)

$\theta_{JA}$ ,  $\Psi_{JLn}$ ,  $\Psi_{JPad}$

## THERMAL CHARACTERISTICS

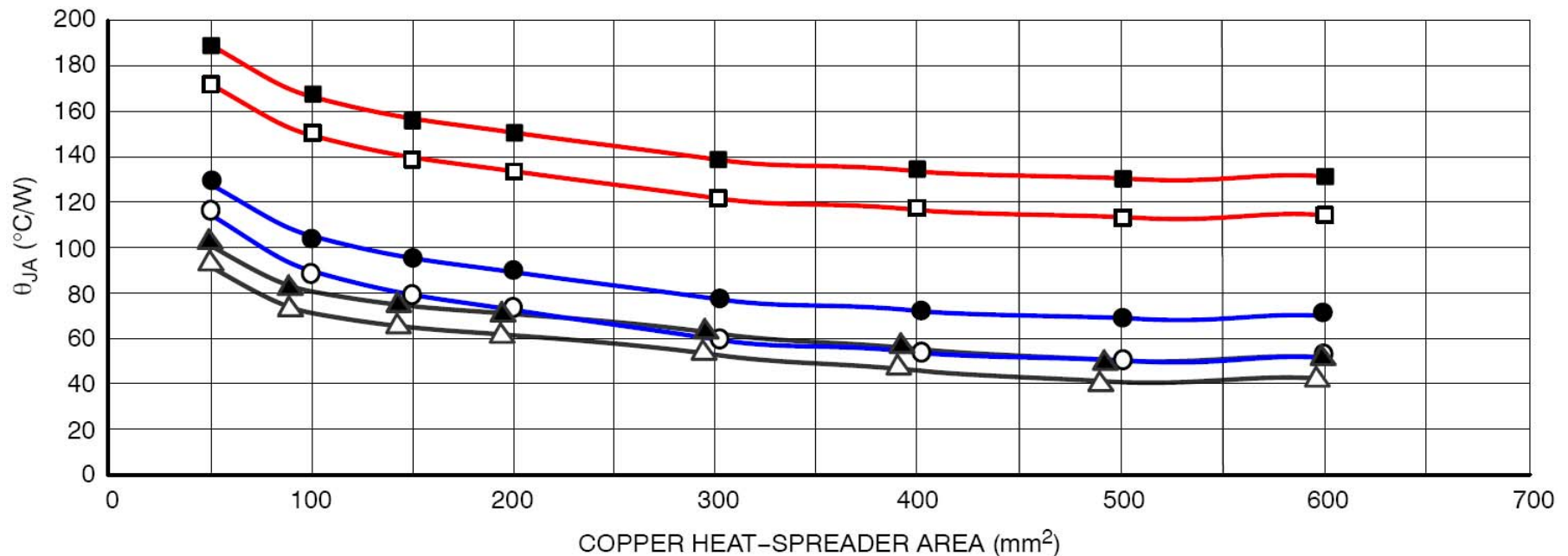
Characteristic	Test Conditions (Typical Values)	Unit
<b>SO-8 Package (Note 5)</b>		
Junction-to-Pin 4 ( $\Psi - JL4$ , $\Psi_{L4}$ )	53.8	°C/W
Junction-to-Ambient Thermal Resistance ( $R_{\theta JA}$ , $\theta_{JA}$ )	170.9	°C/W
<b>SO-8 EP Package (Note 5)</b>		
Junction-to-Pin 8 ( $\Psi - JL8$ , $\Psi_{L8}$ )	23.7	°C/W
Junction-to-Ambient Thermal Resistance ( $R_{\theta JA}$ , $\theta_{JA}$ )	71.4	°C/W
Junction-to-Pad ( $\Psi - JPad$ )	7.7	°C/W
<b>SO-14 Package (Note 5)</b>		
Junction-to-Pin 4 ( $\Psi - JL4$ , $\Psi_{L4}$ )	18.4	°C/W
Junction-to-Ambient Thermal Resistance ( $R_{\theta JA}$ , $\theta_{JA}$ )	111.6	°C/W
<b>SO-20 Package (Note 5)</b>		
Junction-to-Pin 4 ( $\Psi - JL4$ , $\Psi_{L4}$ )	21.8	°C/W
Junction-to-Ambient Thermal Resistance ( $R_{\theta JA}$ , $\theta_{JA}$ )	95.3	°C/W

5. 2 oz copper, 50 mm<sup>2</sup> copper area, 1.5 mm thick FR4

The  $\theta$  and  $\Psi$  values are specified for particular application conditions (PCB parameters). Search in Application Section for other PCB parameters values, i.e.  $\theta_{JA}$  vs PCB area.

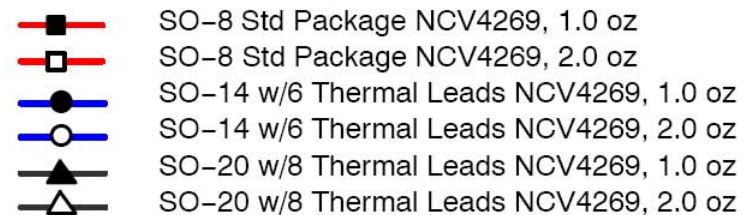
# Thermal Parameters in Datasheet (NCV4269)

## $\theta_{JA}$ vs PCB area



For given package the  $\theta_{JA}$  decreases:

- with increased PCB area
- with increased Cu thickness



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# Suitable Packages for Good Thermal Performance



# Selecting Suitable Package

There is no ideal option. There are always trade-offs among Thermal Performance, PCB footprint size and Cost.

To choose package with sufficient thermal performance, consider mainly:

- Power dissipation (Steady state and pulsed)
- PCB parameters (Area, Cu thickness, Number of layers)
- Temperatures in particular points (Ambient, PCB)

If the package cost is a key factor, try to consider:

- Eliminating other heat sources on PCB which will effectively increase temperature of the PCB
- Using multilayer PCBs larger copper areas and thicker Cu layers. Use thermal vias to improve PCB thermal performance



# LDO Packages Relative Performance Comparison

Package Type	Thermal Performance	PCB footprint	Cost
D2PAK (3, 5, 7 leads + Tab)	++	--	-
DPAK (3, 5 leads including Tab)	++	-	-
SOT-223 (3 leads + Tab)	+	-	+
SO NB (8 leads)	--	+	++
SO NB Fused Leads (8 leads)	-	+	+
SO EP (8 leads + Exposed Pad )	+	+	--
SO NB Fused Leads (14 leads)	-	-	+
SO EP (16 leads + Exposed Pad)	+	--	--
SO WB Fused Leads (16, 20 leads)	-	--	-
Micro8 (8 leads)	--	++	+
TSOP, SOT-23 (5, 6 leads)	--	++	++
DFN (6, 8, 10, 20 leads + Exposed Pad)	+	++	-

+ means relative advantage

- means relative disadvantage

NB – Narrow Body

WB – Wide Body

EP – Exposed Pad (At bottom side of package)

Fused Leads – Leads connected to the leadframe



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# Thermal Calculators for LDOs



## Disclaimer

- These tools do not provide “guaranteed” results since real application conditions are different in most cases (i.e. PCB routing) and this factor has influence on results. There could also be other factors in real applications such as airflow, other heat sources, etc which affect the thermal behavior.
- These tools serve as a guide to show directions for proper thermal design. The models are limited for certain range of operating conditions (i.e. PCB area)





# Thermal Calculator Important Facts

- PCB Cu Area
  - The area number units are mm<sup>2</sup>
  - The larger is area the lower is thermal resistance
- PCB Cu Thickness
  - The thickness units are oz (1 oz is 35 µm, 2 oz is 70 µm)
  - The thicker is Cu layer the lower is thermal resistance
- The Single Layer PCB model is used
- Ambient Temperature, Power, Pulse Width and Duty Cycle can be varied to see effect on Junction Temperature
- Results can be viewed for multiple packages if it is applicable for particular parts



# Thermal Calculator Example (NCV4269)

Package SOIC-14 w/ 6 thermal leads  
Device analog  
Product NCV4269

active area		
Die thk		mm
Die X		mm
Die Y		mm
Die attach Thick		mm
Die Attach Cond		W/MK
PCB Cu Area	50.0	mm^2
PCB Cu thk	1.0	oz
T_junction MAX	150.0	°C
T_ambient	25.0	°C
Power	0.8	W
Pulse ON Time	0.3	sec
Duty Cycle	10%	
Theta JA	127.1	C/W
Psi LA	111.0	C/W
Psi B-A	105.5	C/W
Psi B-top-A	87.7	C/W
Psi J-B-top	39.5	C/W
Psi J-L	16.1	C/W
Tjunc (DC)	126.7	°C
R(0.3sec)	0.0	C/W
Tjunc (single pulse)	25.0	°C
R(0.3sec, 10.0%)	0.0	C/W
Tjunc (pulsed)	25.0	°C

mils  
mils  
sqmils  
mils

Rth C/W

Copper area and Copper thickness curve fit coeff.

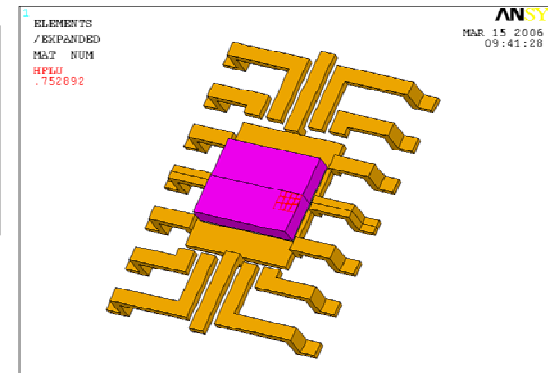
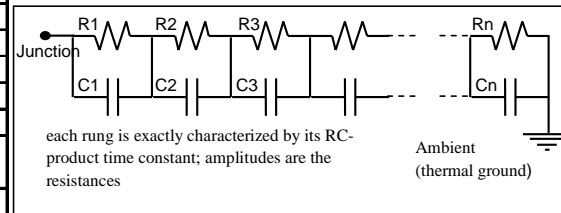
Theta JA Psi LA

	Theta JA	Psi LA	Psi B-A	Psi B-top-A	tau_9	tau_10	tau_10
	LN fit	LN fit	LN fit	LN fit	R_Ln	R_Ln	R_Ln
C	297.17	337.09	361.93	265.84	22.01	27.44	40.05
m1	-0.220117	-0.2840	-0.3151	-0.2836	-0.2049	0.1576	0.0804
m2	-0.190036	-0.2512	-0.2376	-0.2319	0	0	0
R^2	97%	97%	97%	98%	100%	99%	99%

125.6 111.0 105.5 87.7 9.9 50.8 54.8

Ln fit = C\*Cu\_area^m1\*Cu\_oz^m2\*Pl\_thk^m3

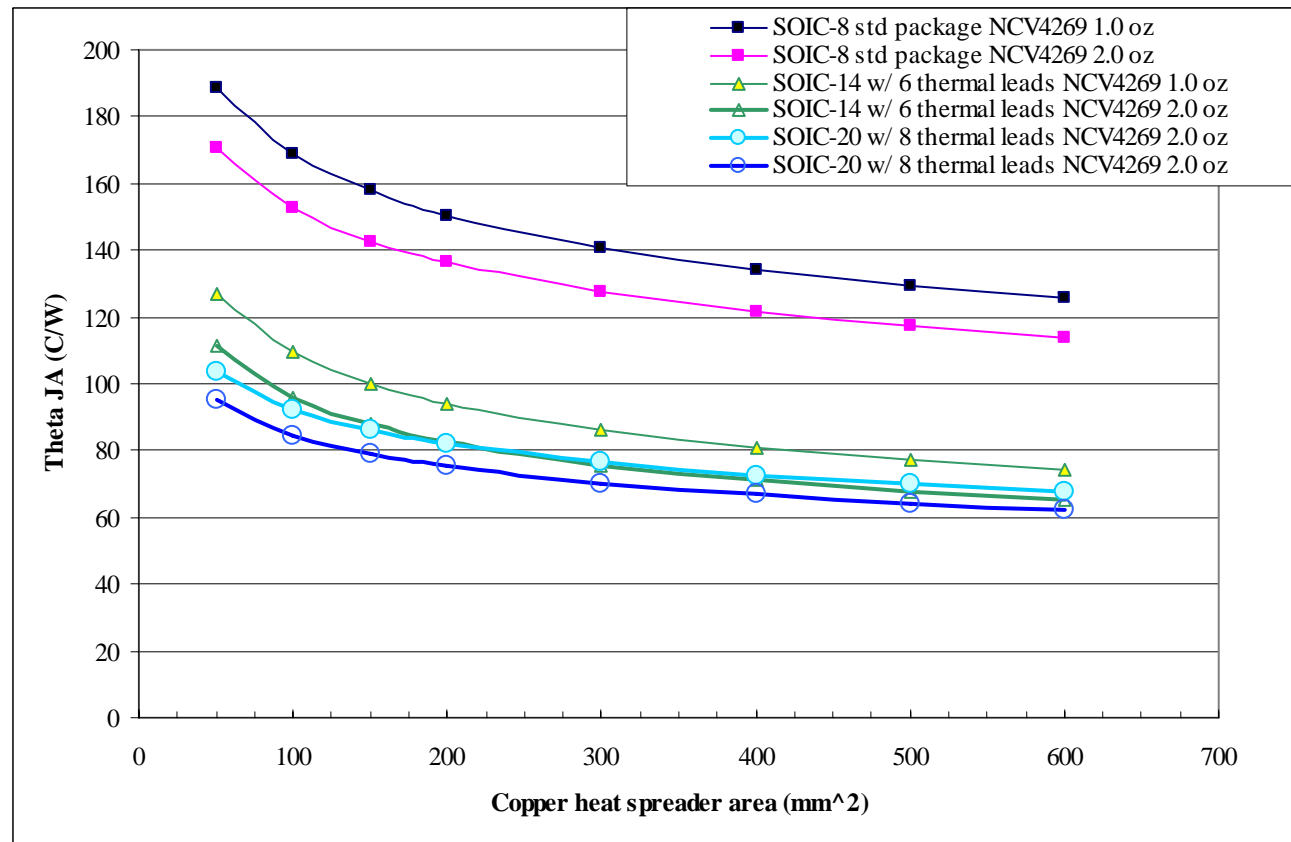
Foster Network



Foster Network	Theta JA	Psi L-A	C (calculated)	Psi L-A	C (calculated)
	R	R		R	
	C/W	C/W		C/W	
	Tau	Tau		Tau	
	Sec	Sec		Sec	
	W-Sec/C	W-Sec/C		W-Sec/C	
1	0.089	1.0E-06	1.1E-05		
2	0.192	1.0E-05	5.2E-05		
3	0.608	1.0E-04	1.6E-04		
4	1.155	5.3E-04	4.6E-04		
5	3.64	0.004	1.1E-03	-0.45	0.023
6	3.10	0.028	9.0E-03	1.20	0.095
7	0.80	0.200	2.5E-01	8.80	1.45
8	10.0	0.45	4.5E-02	27.00	14.40
9	29.0	9.87	3.4E-01	-21.00	48.00
10	77.0	50.8	6.6E-01	95.44	54.85



# Thermal Calculator Results (NCV4269)



# Thermal Calculator File (NCV4269)



NCV4269 Thermal  
Calculator



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# Thermal Simulations used in Silicon Design Phase

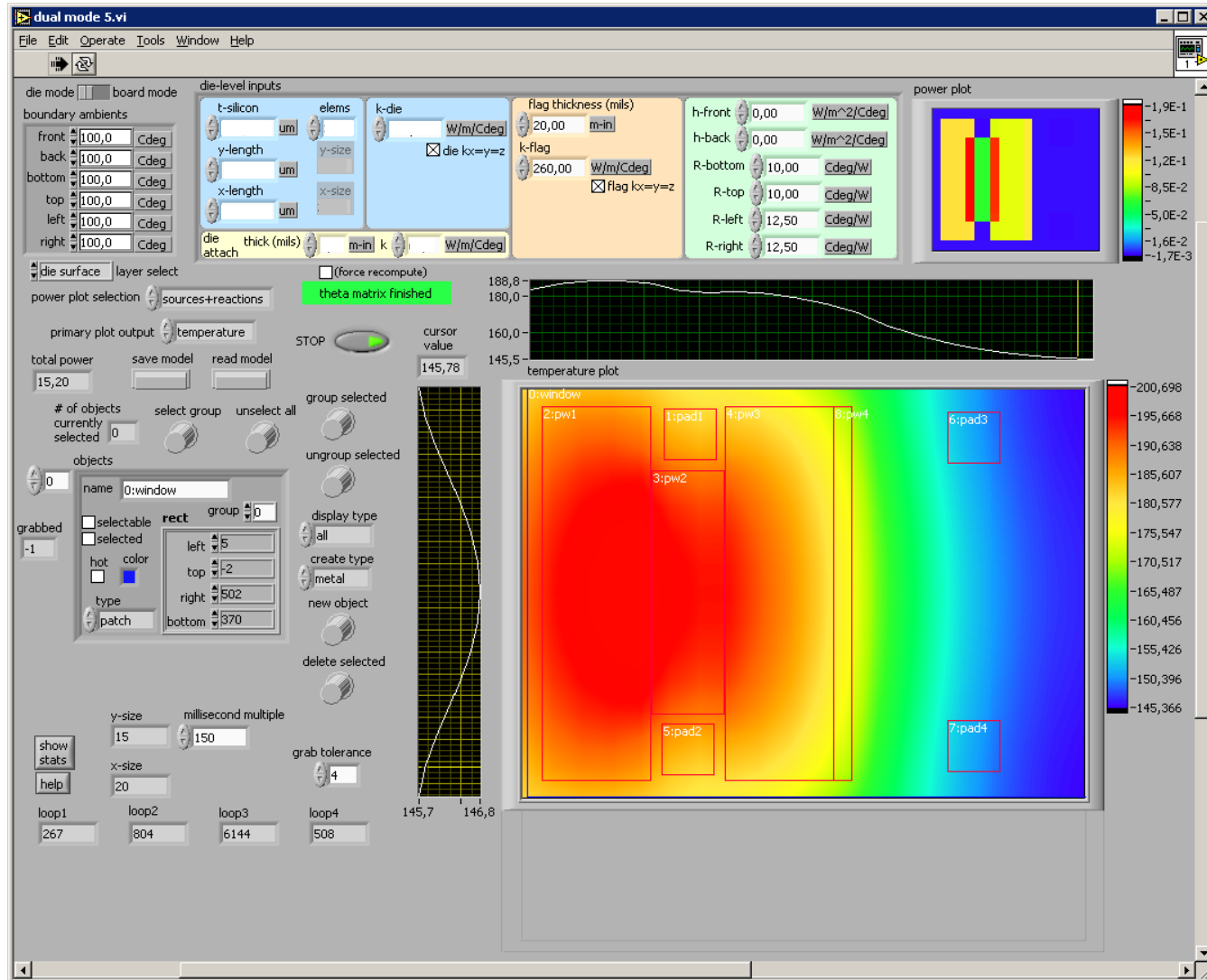


# Thermal Simulation Tools at Silicon (Die) Level

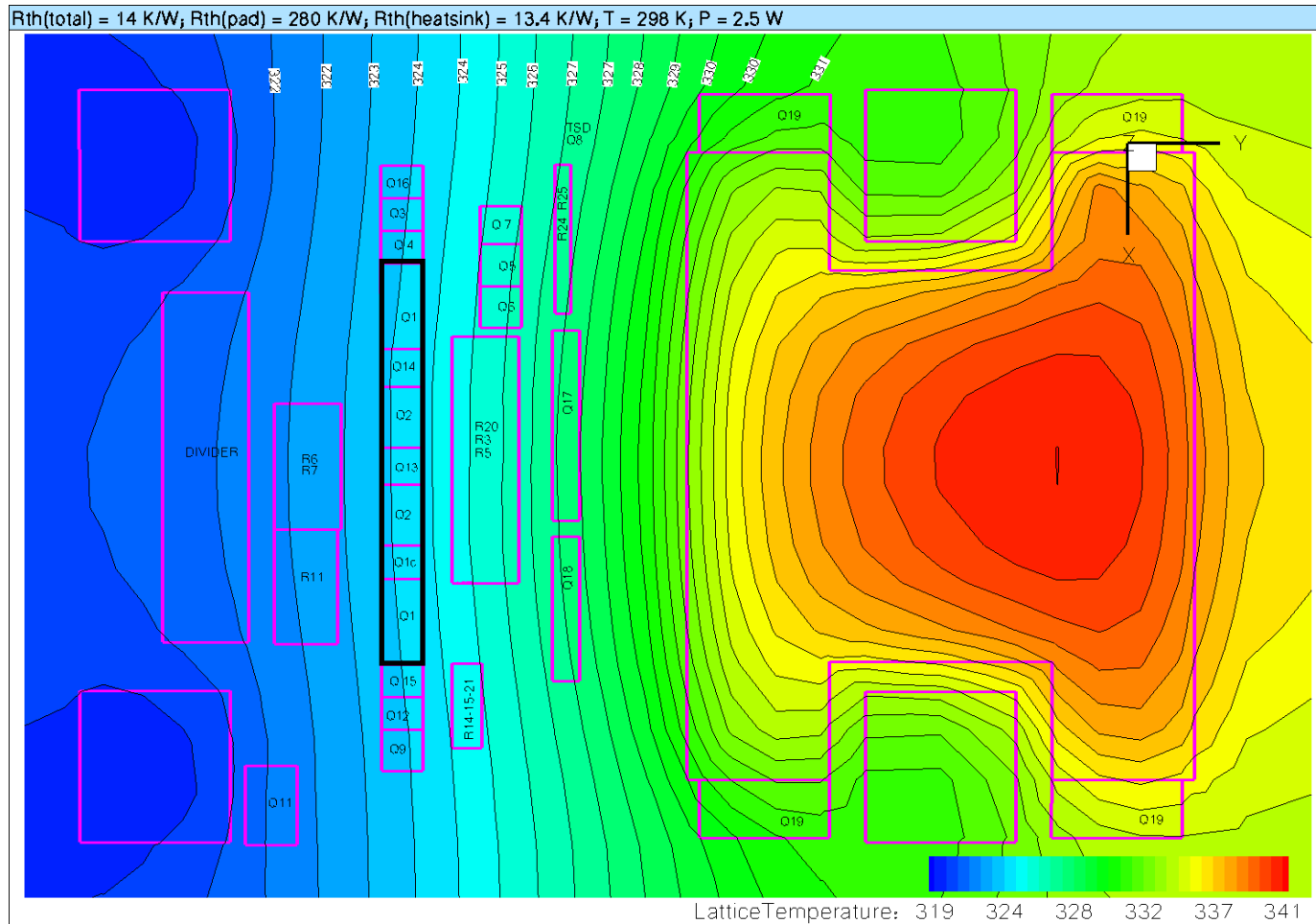
- The tools are important to predict thermal behavior of Silicon and provide guidelines for proper design and layout, mainly for temperature sensitive circuitries
- Three possible simulation tools in Silicon Design phase
  - Thermal Tool
    - Steady-state **thermal** simulations
    - Three-layer die level simulation, linear system
    - LabView environment
  - Synopsys TCAD
    - Steady-state as well as transient **thermal** simulations
    - Nonlinear system, calculations based on the finite element method (FEM)
  - HeatWave
    - Steady-state, transient, thermal and **electro-thermal** simulations
    - Nonlinear system, calculations based on the finite element method (FEM)
    - The most precise and the most complex calculations



# Thermal Tool

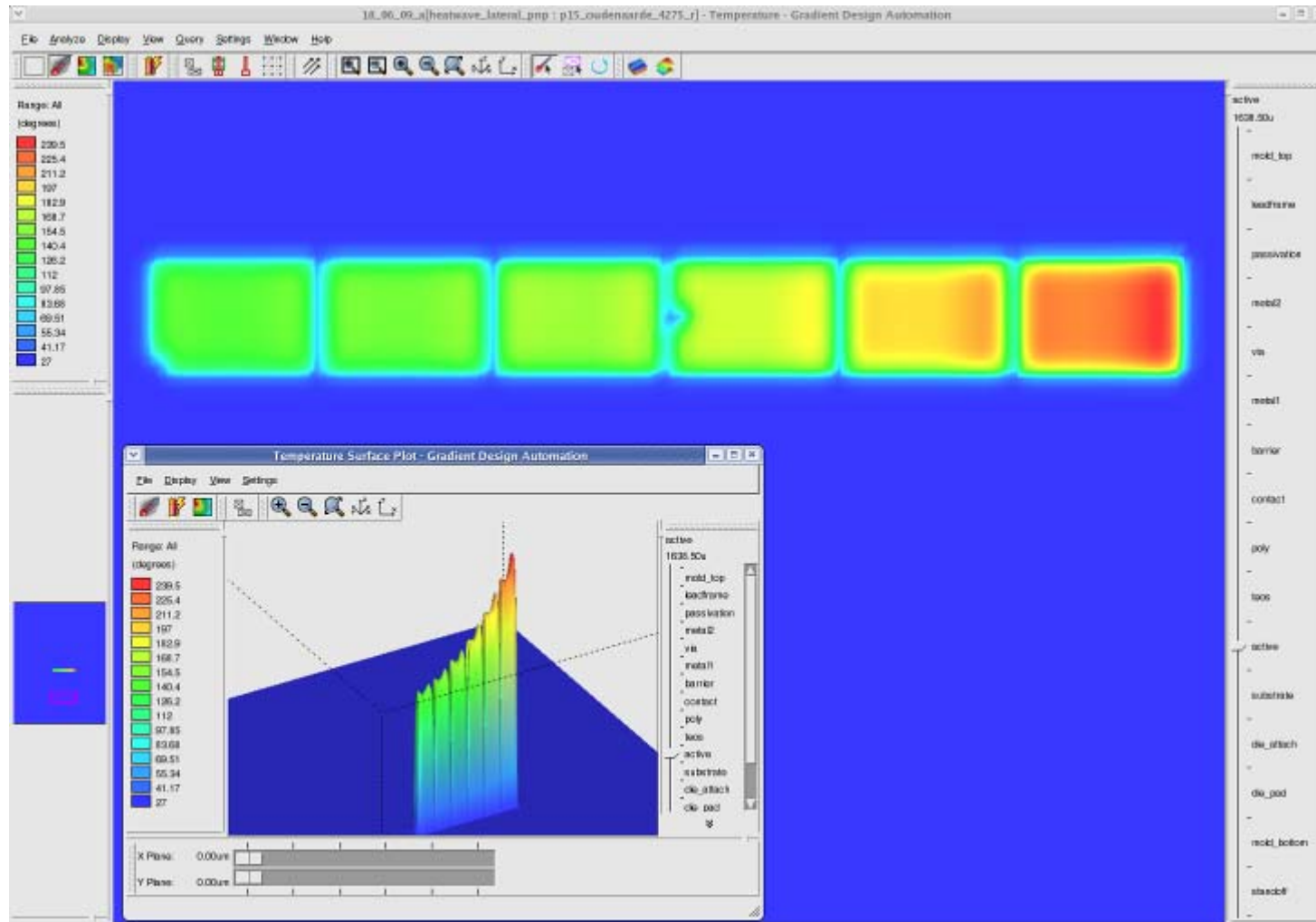


# Synopsys TCAD





# HeatWave



## References

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2. Psi or Theta: Which One Should You Choose? (Article in Power Electronics Technology, May 2008), Roger Stout, P.E., ON Semiconductor
3. Application Note: AND8220/D How To Use Thermal Data Found in Data Sheets  
[http://www.onsemi.com/pub\\_link/Collateral/AND8220-D.PDF](http://www.onsemi.com/pub_link/Collateral/AND8220-D.PDF)
4. Thermal Simulations (Presentation 1<sup>st</sup> July 2009), Andrej Vrbicky, Bratislava Development Center, ON Semiconductor
5. Website <http://www.jedec.org/>



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## For More Information

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